DSP Implementation of Output Voltage Reconstruction in CSI-Based Converters

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***Abstract*— Current-source-inverter-based uninterruptible power supplies and V/f-controlled induction motor drives require sensing of two or more load voltages in addition to the dc voltage sensors used for protection purposes. This paper proposes a digital-signal-processor (DSP)-based load voltage control scheme that requires only information provided by the dc-bus voltage sensor. Load voltage estimation is based on ac line voltage reconstruction by means of a recursive least-square error algorithm that uses the information available on the dc bus and knowledge of the pulsewidth modulation gating pattern. Thus, the system minimizes the transducer count and, therefore, enhances reliability and ruggedness. Experimental results show that the load voltage can be reconstructed and its rms value controlled for a wide range of operating conditions with errors of at most 4%. Moreover, the use of the space-vector modulation technique ensures a reduced load voltage harmonic distortion, which remains within the 5% range at nominal voltage and for all load conditions. The paper presents the DSP algorithms required for the operation of the system and key experimental results obtained on a three-phase 208-V 60-Hz 2-kVA prototype unit.**

***Index Terms*— Current-source inverter, space-vector pulsewidth modulation, voltage control, voltage reconstruction.**

I. Introduction

THE most common three-phase power supplies use topologies based on an intermediate dc link and on the voltage-source inverter (VSI) topology [1]. The VSI implementation is simple because the power circuit can be operated over the full load frequency/voltage range without major restrictions on the gating signals and consideration of the nature of the load. However, the VSI has intrinsic weaknesses, among which is the high dv/dt waveforms applied to the load. Furthermore, sustained power regeneration is not possible when a diode bridge front-end rectifier is used.

Current-source inverter (CSI) topologies, on the other hand, apply sinusoidal voltages to the load [2]. However, restrictions are imposed to the gating patterns, which can be met with a fixed pattern [3]–[5]. Although the output current pattern can be optimized, transient response in this case is slow, since the dc-link current has to be varied [6]. However, on-line current pulsewidth modulation (PWM) pattern generation can be implemented with appropriate gating interface circuits [7], [8]. The load voltage can then be precisely shaped and regulated [9]. This gives the CSI a voltage-source characteristic, with the additional advantages of inherent current limiting and low load voltage harmonic distortion. The converter can, therefore, be used for uninterruptible power supply (UPS) applications or V/f-controlled induction motor drives.

In an attempt to reduce the number of current sensors, load current reconstruction has been proposed for VSI's [10]–[12]. Applying the duality principle, it is possible to reconstruct the load voltages in a CSI. This reduces the number of voltage sensors in current-source-based dc-link converters, which normally require two or more load voltage transducers, in addition to the dc voltage sensor used for protection purposes.

This paper proposes a digital signal processor (DSP) based voltage control scheme that requires only information provided by the dc-bus voltage sensor. Load voltage estimation is based on ac line voltage reconstruction by means of information available on the dc bus and knowledge of the PWM gating pattern. To achieve this, the CSI dc-link voltage is sampled and, in combination with the gating information of the switches, is used to reconstruct the load voltage waveforms. A corresponding load rms voltage is computed and used as a feedback variable to control on a continuous basis the load voltage. The resulting system minimizes the transducer count, which enhances system ruggedness. Moreover, the use of the space-vector modulation (SVM) technique results in reduced load voltage harmonic distortion for all operating conditions, including no-load operation. This paper presents the DSP algorithms required for the operation of the system. Experimental results on a three-phase 208-V 60-Hz 2-kVA prototype inverter are included to demonstrate the feasibility of the algorithms and evaluate the static and transient performance of the system.

II. Description and Operation of the Three-Phase CSI-Based System

A. Power Circuit

The power circuit (Fig. 1) is composed of a dc-link reactor $(L_{\rm dc})$, a three-phase PWM CSI, and a three-phase capacitive filter (C_o). The load is a passive RL load. DC-link current control is obtained by means of a thyristor rectifier.

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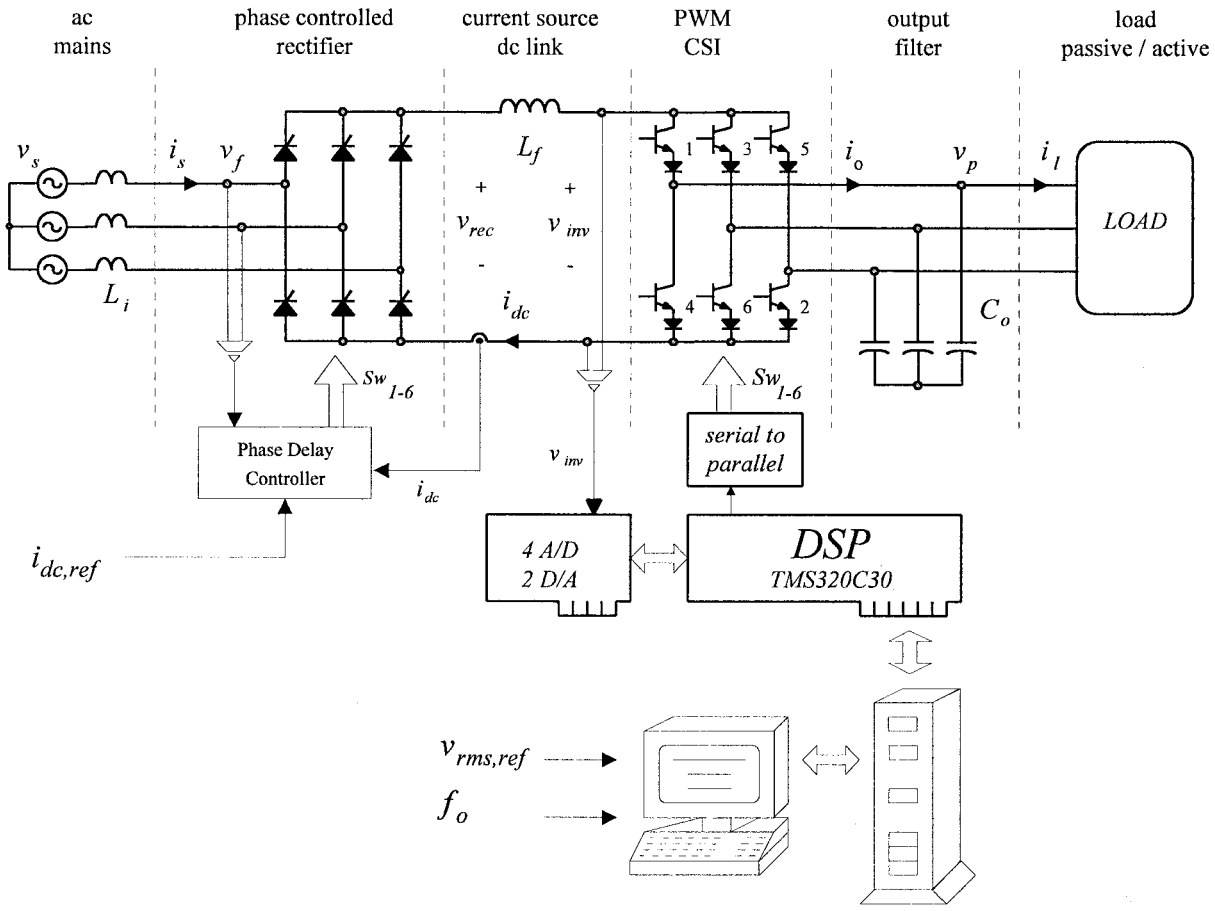


Fig. 1. Power circuit of a PWM CSI-based power supply system.

The thyristor rectifier regulates the level of the dc-link current $(i_{\rm dc})$, by adjusting the dc rectifier voltage $(v_{\rm rec})$. In steady state, the dc rectifier voltage $(v_{\rm rec})$ equals the dc CSI voltage $(v_{\rm inv})$. The dc-link reactor $(L_{\rm dc})$ absorbs the voltage harmonics produced by the phase control operation of the rectifier and the PWM operation of the CSI. Therefore, the combination of both the thyristor rectifier and the dc-link inductor appears as a current source to the CSI. The main function of the CSI is to produce three-phase PWM line currents (i_o), with minimum harmonic distortion. The implementation of PWM techniques in CSI's requires unidirectional switches with reverse-blocking voltage capabilities, such as the diode–bipolar junction transistor (BJT) combination. Finally, the capacitive load filter (C_o) absorbs the current harmonics generated by the PWM CSI operation and defines the sinusoidal voltages applied to the load.

B. Control System

The control strategy (Fig. 2) is based on two independent loops: 1) the rms load voltage $(v_{\rm rms})$ and 2) the dc-link current $(i_{\rm dc})$ loops. The rms load voltage control loop [Fig. 2(a)] is entirely implemented by means of a TMS320C30-based DSP system (Fig. 1). A *proportional integral (PI) control algorithm* sets the modulation index of the CSI $(M_{\rm inv})$ such that the rms load voltage $(\hat{v}_{\rm rms})$ is equal to the rms load voltage reference $(v_{\rm rms,\,ref})$. The modulation index $(M_{\rm inv})$ and the desired load frequency (f_o) are used by the *SVM algorithm* to produce the gating signals applied to the CSI $(Sw_k,\, k = 1, \cdots, 6)$. The DSP system samples the dc voltage (inverter side, $v_{\rm inv}$) and, by using the available switching information, the *instantaneous line voltage algorithm* and the *line voltage reconstruction algorithm* reconstruct the load voltage waveforms. This last algorithm assumes that the actual load voltages are sinusoidal waveforms of the form $a_i \cdot \cos(2\pi f_o t) + b_i \cdot \sin(2\pi f_o t)$ and calculates the coefficients $\hat{\Theta}_i = [a_i\ b_i]^T\ (i = 1, 2, 3)$ based on a recursive least-square error (RLSE) approximation method [13]. Finally, the *rms voltage estimation algorithm* uses the coefficients $\hat{\theta}_i$ to derive on a continuous basis the rms load voltage $(\hat{v}_{\rm rms})$. These algorithms are further explained in the next section.

The second control loop is the dc-link current control [$i_{\rm dc}$, Fig. 2(b)]. The associated control circuitry is implemented using an analog approach. A PI controller sets the delay angle (α) such that the dc-link current $(i_{\rm dc})$ is equal to the dc-link current reference $(i_{\rm dc,\,ref})$. In other words, the rectifier produces a dc voltage $(v_{\rm rec})$ that, in steady state, always matches the dc voltage produced by the CSI PWM operation $(v_{\rm inv})$.

III. Load Voltage Reconstruction

To control on a continuous basis the rms load voltage, an RLSE algorithm is used to reconstruct the load voltage

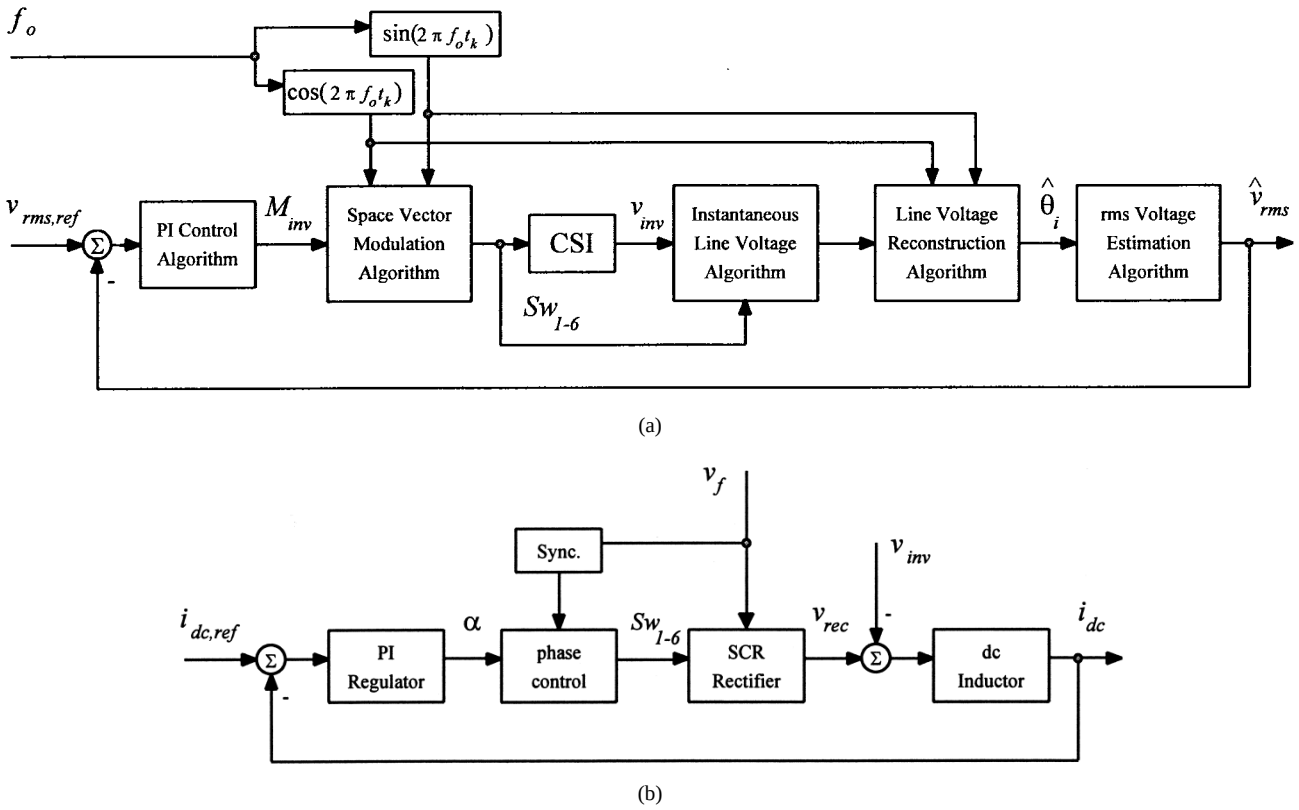


Fig. 2. Block diagram representation of the power supply control strategy: (a) load rms voltage control loop and (b) dc-bus current control loop.

waveforms and an averaging algorithm to derive the rms load voltage at every sample instant. This quantity is then used in the feedback loop [Fig. 2(a)].

A. Formulation of the LSE

The data available are the sampled voltage on the dc-link CSI side (v_{inv}), the available switching state information (Sw_k, $k = 1, \cdots, 6$), and the space-vector sinusoidal templates [Fig. 2(a)]. The actual load voltages are assumed to be of the form

$$\hat{y}_1(t_k) = \hat{v}_{ab}(t_k) = a_1 \cos(2\pi f_o t_k) + b_1 \sin(2\pi f_o t_k) \quad (1)$$
$$\hat{y}_2(t_k) = \hat{v}_{bc}(t_k) = a_2 \cos(2\pi f_o t_k) + b_2 \sin(2\pi f_o t_k) \quad (2)$$
$$\hat{y}_3(t_k) = \hat{v}_{ca}(t_k) = a_3 \cos(2\pi f_o t_k) + b_3 \sin(2\pi f_o t_k) \quad (3)$$

where

$\hat{y}_i(t_k)$	reconstructed load voltages ($i = 1, 2, 3$);
$\hat{\theta}_i = [a_i \;\; b_i]^T$	coefficients to identify;
$\sin(2\pi f_o t_k)$, $\cos(2\pi f_o t_k)$	sinusoidal templates (f_o: load frequency).

The *instantaneous line voltage algorithm* assumes zero load voltages as initial conditions ($v_{ab}(t_k) = 0$, $v_{bc}(t_k) = 0$, and $v_{ca}(t_k) = 0$). On the other hand, the sampled dc-bus voltage at the instant $t_k(v_{\text{inv}}(t_k))$ corresponds to one of the actual load line-to-line voltages according to the status (ON or OFF) of the CSI switches. This assignation, which is also implemented in the *instantaneous line voltage algorithm* in Fig. 2(a), is as follows:

$$\text{if}((Sw_1{=}{=}\text{on})\&\&(Sw_2{=}{=}\text{on}))\, v_{ca}(t_k) = -v_{\text{inv}}(t_k);$$
$$\text{if}((Sw_2{=}{=}\text{on})\&\&(Sw_3{=}{=}\text{on}))\, v_{bc}(t_k) = v_{\text{inv}}(t_k);$$
$$\text{if}((Sw_3{=}{=}\text{on})\&\&(Sw_4{=}{=}\text{on}))\, v_{ab}(t_k) = -v_{\text{inv}}(t_k);$$
$$\text{if}((Sw_4{=}{=}\text{on})\&\&(Sw_5{=}{=}\text{on}))\, v_{ca}(t_k) = v_{\text{inv}}(t_k);$$
$$\text{if}((Sw_5{=}{=}\text{on})\&\&(Sw_6{=}{=}\text{on}))\, v_{bc}(t_k) = -v_{\text{inv}}(t_k);$$
$$\text{if}((Sw_6{=}{=}\text{on})\&\&(Sw_1{=}{=}\text{on}))\, v_{ab}(t_k) = v_{\text{inv}}(t_k).$$

Given the absence of information, the two voltages that remain equal to zero are approximated by (1)–(3) (whichever applies) in a last stage of the *instantaneous line voltage algorithm*. For instance, if Sw_1 and Sw_2 are ON, then $v_{ca}(t_k) = -v_{\text{inv}}(t_k)$, and $v_{ab}(t_k)$ and $v_{bc}(t_k)$ remain equal to zero, which are approximated using (1) and (2). In this case, the last stage of the algorithm uses the coefficients a_1, b_1, a_2, and b_2 obtained in the sample instant t_{k-1}. If all the switches are OFF, then the identification process is skipped and the rms load voltage loop is implemented based on the rms load voltage obtained in the sample instant t_{k-1}.

The voltages $v_{ab}(t_k)$, $v_{bc}(t_k)$, and $v_{ca}(t_k)$ are the actual pieces of the load voltages, and they are conveniently represented by

$$y_1(t_k) = v_{ab}(t_k) \quad (4)$$
$$y_2(t_k) = v_{bc}(t_k) \quad (5)$$
$$y_3(t_k) = v_{ca}(t_k). \quad (6)$$

On the other hand, the reconstructed load voltages (1)–(3) can be written as

$$\hat{y}_i(t_k) = \mathbf{N}^T(t_k)\hat{\theta}_i(t_k) \tag{7}$$

where $\mathbf{N}^T(t_k) = [\cos(2\pi f_o t_k)\ \sin(2\pi f_o t_k)]$.

After N samples, the reconstructed load voltages (7) can be written as

$$\hat{\mathbf{Y}}_i(t_N) = \mathbf{M}(t_N)\hat{\theta}_i(t_N) \tag{8}$$

where $\hat{\mathbf{Y}}_i(t_N) = [\hat{y}_i(t_1)\ \cdots\ \hat{y}_i(t_N)]^T$ and $\mathbf{M}(t_N) = [\mathbf{N}^T(t_1)\ \cdots\ \mathbf{N}^T(t_N)]^T$. Also, after N samples, the actual load voltages can be expressed as

$$\mathbf{Y}_i(t_N) = [y_i(t_1)\ \cdots\ y_i(t_N)]^T. \tag{9}$$

In Appendix A, the LSE solution of (8) that includes the weighting matrix $\mathbf{W}(t_N)$ is derived [13]. Thus, the resulting expression for the coefficients $\hat{\theta}_i(t_N)$ after N samples is

$$\hat{\theta}_i(t_N) = \{\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N)\}^{-1} \times \mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{Y}_i(t_N). \tag{10}$$

The weighting matrix $\mathbf{W}(t_N)$ defines the dynamic response or tracking capability of the identification algorithm [13]. An alternative form to allow fast response is to weight more the latest data. Thus, $\mathbf{W}(t_N)$ is chosen of the form

$$\mathbf{W}(t_N) = \begin{bmatrix} \lambda^{N-1} & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & \lambda^1 & 0 \\ 0 & \cdots & 0 & 1 \end{bmatrix} \tag{11}$$

where λ is the forgetting factor and must be $0 < \lambda \leq 1$. Note that $\lambda = 1$ implies that all the sampled data are equally weighted, and $\lambda < 1$ that only the latest data is used.

In real-time applications, the expression for the coefficients (10) can be further simplified if $\mathbf{M}(t_N)$ and $\mathbf{W}(t_N)$ are fixed. This is the case when the number of samples (N), the forgetting factor (λ), and the load frequency (f_o) are not time dependent. Under these conditions, the factor $\{\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N)\}^{-1}\mathbf{M}^T(t_N)\mathbf{W}(t_N)$ becomes constant and, therefore, could be precalculated and stored off-line. Thus, (10) could be solved on-line with a minimum number of operations. However, the above conditions are not present in the proposed applications (i.e., when the number of samples (N) or the load frequency (f_o) are changed during operation). Therefore, an RLSE algorithm is preferred. Thus, (10) is solved on-line with a minimum number of operations and without requiring precalculated and stored data.

B. Formulation of the RLSE

In order to find a recursive algorithm to solve (10), the matrices $\mathbf{M}(t_N)$, $\mathbf{Y}_i(t_N)$, and $\mathbf{W}(t_N)$ are arranged as

$$\mathbf{M}(t_N) = \begin{bmatrix} \mathbf{M}(t_{N-1}) \\ \cdots\cdots\cdots \\ \mathbf{N}^T(t_N) \end{bmatrix}$$

$$\mathbf{Y}_i(t_N) = \begin{bmatrix} \mathbf{Y}_i(t_{N-1}) \\ \cdots\cdots\cdots \\ y_i(t_N) \end{bmatrix}$$

$$\mathbf{W}(t_N) = \begin{bmatrix} \lambda\mathbf{W}(t_{N-1}) & \vdots & 0 \\ \cdots\cdots\cdots\cdots & \vdots & \cdots \\ 0^T & \vdots & 1 \end{bmatrix}. \tag{12}$$

Replacing (12) in the coefficients expression (10) yields

$$\hat{\theta}_i(t_N) = \{\lambda\mathbf{M}^T(t_{N-1})\mathbf{W}(t_{N-1})\mathbf{M}(t_{N-1}) + \mathbf{N}(t_N)\mathbf{N}^T(t_N)\}^{-1} \times \{\lambda\mathbf{M}^T(t_{N-1})\mathbf{W}(t_{N-1})\mathbf{Y}_i(t_{N-1}) + \mathbf{N}(t_N)y_i(t_N)\}. \tag{13}$$

In addition, the propagation matrix $\mathbf{P}(t_N)$ is defined as $\mathbf{P}(t_N) = (\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N))^{-1}$. Thus, the coefficients (10) can also be written as

$$\hat{\theta}_i(t_N) = \mathbf{P}(t_N)\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{Y}_i(t_N) \tag{14}$$

and from (13), it is found that

$$\mathbf{P}^{-1}(t_N) = \lambda\mathbf{P}^{-1}(t_{N-1}) + \mathbf{N}(t_N)\mathbf{N}^T(t_N). \tag{15}$$

Thus, using (14) and (15), the coefficients (13) can be expressed as

$$\hat{\theta}_i(t_N) = \hat{\theta}_i(t_{N-1}) + \mathbf{P}(t_N)\mathbf{N}(t_N)\{y_i(t_N) - \mathbf{N}^T(t_N)\hat{\theta}_i(t_{N-1})\}. \tag{16}$$

The resulting expression (16) is a recursive expression on $\hat{\theta}_i$ which requires the matrix $\mathbf{P}(t_N)$; therefore, the inverse of the matrix $\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N)$ at every sample instant should be calculated. Fortunately, this operation is avoided since $\mathbf{P}(t_N)$ can also be expressed recursively (Appendix B) as

$$\mathbf{P}(t_N) = \left\{\mathbf{P}(t_{N-1}) - \frac{\mathbf{P}(t_{N-1})\mathbf{N}(t_N)\mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})}{\lambda + \mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})\mathbf{N}(t_N)}\right\}\frac{1}{\lambda}. \tag{17}$$

Finally, using (17), the coefficients (16), implemented in the *line voltage reconstruction algorithm* in Fig. 2(a), are

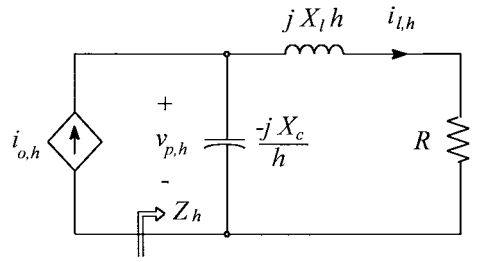
$$\hat{\theta}_i(t_N) = \hat{\theta}_i(t_{N-1}) + \frac{\mathbf{P}(t_{N-1})\mathbf{N}(t_N)}{\lambda + \mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})\mathbf{N}(t_N)} \times \{y_i(t_N) - \mathbf{N}^T(t_N)\hat{\theta}_i(t_{N-1})\}. \tag{18}$$

The forgetting factor λ defines the weighting matrix $\mathbf{W}(t_N)$ and, thereby, the stability and the speed of the identification algorithm [13]. In fact, a high value $(\lambda = 1)$ provides good stability; however, the algorithm has poor tracking capabilities. Therefore, stability and dynamic response as a function of λ are important design issues which are experimentally addressed in Section VI.

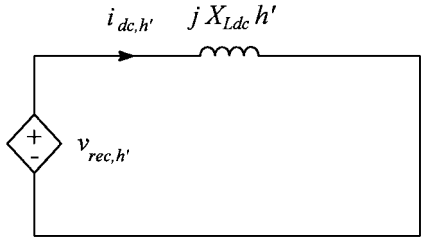
C. Formulation of the RMS Voltage

To control on a continuous basis the rms value of a sinusoidal waveform [such as (1)–(3)], an instantaneous rms quantity is introduced. Thus, the rms value of each reconstructed component $(\hat{y}_{i,\mathrm{rms}})$ based on the coefficients $\hat{\theta}_i = [a_i\ b_i]^T (i = 1, 2, 3)$ is defined as

$$\hat{y}_{i,\mathrm{rms}} = \frac{\sqrt{a_i^2 + b_i^2}}{\sqrt{2}}. \tag{19}$$



(a)



(b)

Fig. 3. Equivalent circuits: (a) CSI ac side including capacitive filter and load and (b) dc-link model for $h' = 6, 12, \cdots, < f_{sw}/f_o$.

Therefore, the actual instantaneous rms load voltage $(\hat{v}_{\rm rms})$ based on the above expression, implemented in the *rms voltage estimation algorithm* in Fig. 2(a), can be defined as

$$\hat{v}_{\rm rms} \cong \frac{1}{3} \cdot \sum_{i=1}^{3} \hat{y}_{i,\,\rm rms} = \frac{1}{3} \cdot \sum_{i=1}^{3} \frac{\sqrt{a_i^2 + b_i^2}}{\sqrt{2}}. \tag{20}$$

IV. Design Guidelines

A. Load Filter Capacitors

These capacitors are designed to achieve a desired load voltage quality by limiting its harmonic peak to a given value. Since the CSI is gated using an SVM, a PWM type of line current pattern is expected. The per-phase model of the CSI ac side and RL load shown in Fig. 3(a) is assumed. Therefore, the normalized impedance of the filter and load for a given harmonic h is

$$|Z_h| = X_c \sqrt{\frac{1 + X_l^2(h^2-1)}{X_c^2 - 2h^2 X_c X_l + h^2 + h^2 X_l (h^2-1)}} \tag{21}$$

and, since the ac CSI line current harmonic can be expressed by $i_{o,\,h} = M_{\rm inv} K_h i_{\rm dc}/\sqrt{2}$, the load phase fundamental voltage component $(h = 1)$ becomes

$$V_{p,\,1} = \frac{M_{\rm inv}}{\sqrt{2}}\, K_1 i_{\rm dc}\, \frac{X_c}{\sqrt{X_c^2 - 2X_c X_l + 1}} \tag{22}$$

and the load phase voltage harmonic components $(V_{p,\,h})$, assuming they are at high frequencies $(h \gg 1)$, are given by

$$V_{p,\,h} = \frac{K_h}{\sqrt{2}}\, i_{\rm dc}\, \frac{X_c}{h} \tag{23}$$

where

- $M_{\rm inv}$ CSI modulation index;
- K_1 ac gain of the PWM technique ($K_1 = 1$ for SVM);
- X_c filter reactance $(X_c = 1/(2\pi f_o C_o))$;
- X_l load reactance $(X_l = 2\pi f_o L_o)$;
- K_h harmonic gain of the PWM controller (function of $M_{\rm inv}$);
- h harmonic order.

To simplify the calculations, a first approximation is to assume that the dominant voltage harmonics $(V_{p,\,h})$ are concentrated at the switching frequency $(f_{sw} = n \cdot f_o)$ and with an equivalent maximum amplitude given by

$$V_{p,\,n} = \frac{i_{\rm dc}}{\sqrt{2}}\, \frac{X_c}{n} \tag{24}$$

where n is the normalized switching frequency. By forcing the load voltage harmonic $V_{p,\,n}$ to be at most equal to $k_{\rm ac}$ of its fundamental (i.e., $V_{p,\,n} = k_{\rm ac} V_{p,\,1}$, where, for instance, $k_{\rm ac} = 0.05$) and by using (22) and (24), the filter reactance is calculated as follows:

$$X_c = X_l + \sqrt{X_l^2 + (k_{\rm ac} M_{\rm inv} K_1 n)^2 - 1}. \tag{25}$$

B. DC-Link Current Reference

The nominal dc-link current reference expression $(i_{\rm dc,\,ref})$ that ensures the operation of the CSI at the given modulation index $(M_{\rm inv})$ can be derived from (22) and (25). Thus,

$$i_{\rm dc,\,ref} = \frac{\sqrt{2}}{M_{\rm inv}}\, \frac{1}{K_1} \sqrt{1 - 2\,\frac{X_l}{X_c} + \frac{1}{X_c^2}}. \tag{26}$$

C. DC-Link Inductor

The thyristor rectifier and dc-link inductor $(L_{\rm dc})$ act as a current source to the CSI. Therefore, the dc-link inductor should be designed to absorb the voltage harmonics produced by both the front-end rectifier and the PWM CSI operation. In practice, it is sufficient in the design to consider the sixth voltage harmonic produced by the thyristor rectifier and neglect the high-frequency harmonics produced by the CSI, due to their limited influence on current harmonics.

Fig. 3(b) shows a simplified equivalent circuit of the dc link. Thus, the sixth harmonic $(h' = 6)$ in the dc current becomes

$$i_{\rm dc,\,6} \cong \frac{1}{6}\, \frac{v_{\rm rec,\,6}}{2\pi f_s L_{\rm dc}}. \tag{27}$$

Therefore,

$$L_{\rm dc} \cong \frac{1}{6}\, \frac{v_{\rm rec,\,6}}{i_{\rm dc,\,6} 2\pi f_s} = \frac{1}{6}\, \frac{k_\alpha V_s}{i_{\rm dc,\,6} 2\pi f_s} \tag{28}$$

where

- k_α constant that depends upon the delay angle (α);
- V_s supply line voltage;
- $i_{\rm dc,\,6}$ sixth current harmonic;
- f_s ac supply frequency ($f_s = 60$ Hz);
- $v_{rec,\,6}$ sixth rectifier voltage harmonic.

Finally, by limiting the sixth current harmonic to be $k_{\rm dc}$ of the dc nominal value (i.e., $i_{\rm dc,\,6} = k_{\rm dc} i_{\rm dc}$, where, for instance, $k_{\rm dc} = 0.1$), it is possible to derive from (28)

$$L_{\rm dc} = \frac{k_\alpha V_s}{12 k_{\rm dc} \pi f_s i_{\rm dc}}. \tag{29}$$

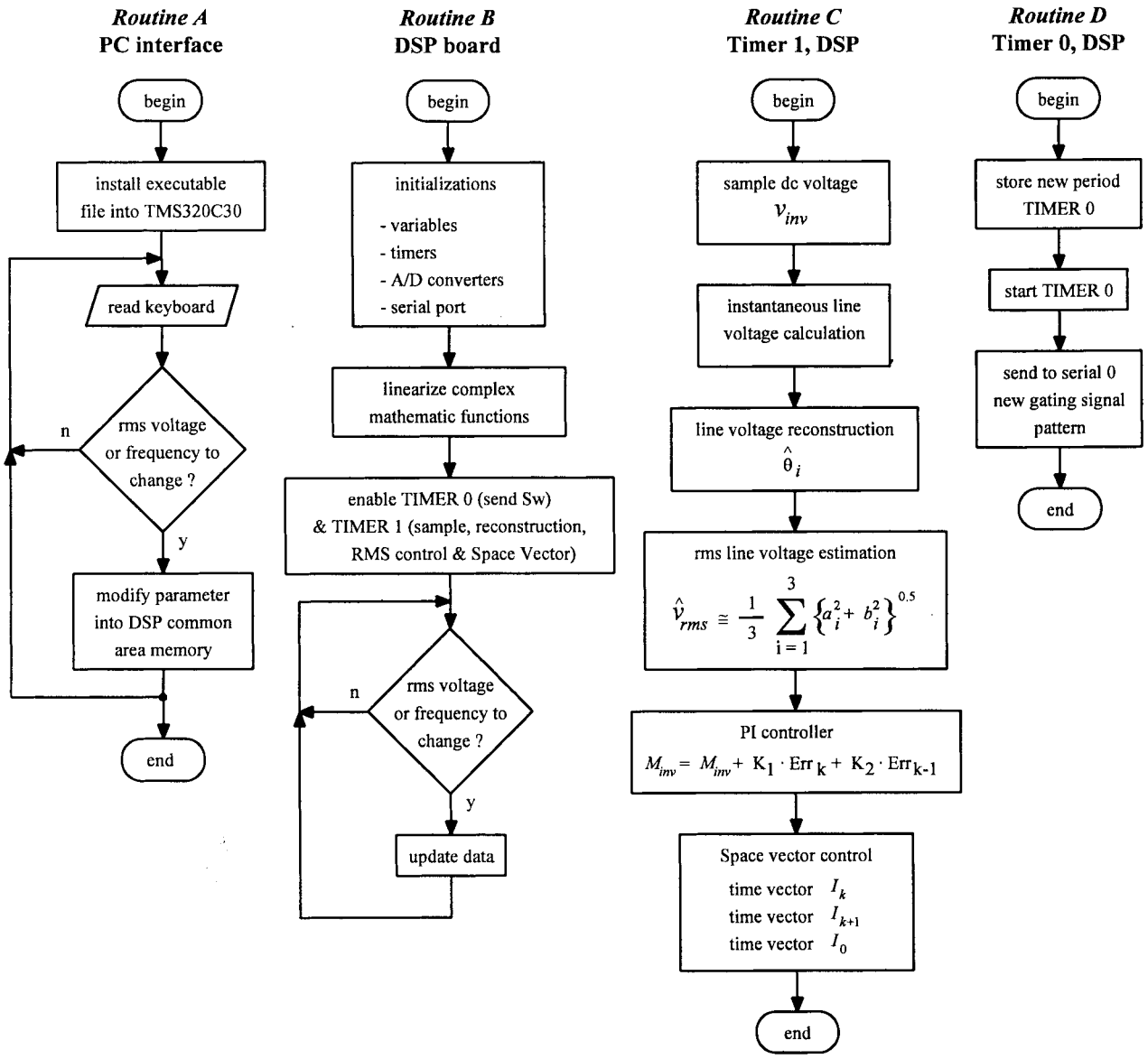


Fig. 4. Flow chart of the algorithms running on the PC and DSP systems.

D. Design Example

To illustrate the use of the design guidelines and equations, a design example is presented. The load specifications are a follows: $S = 2$ kVA, $V = 220$ V, $f_o = 60$ Hz, and $\cos(\phi) = 0.8$ (lagging). Thereby, the base values are as follows: $V_{\text{base}} = 127$ V, $I_{\text{base}} = 5.3$ A, $Z_{\text{base}} = 24.2\ \Omega$, and $f_{\text{base}} = 60$ Hz. The converter operates at the nominal modulation index $M_{\text{inv}} = 0.8$. With this value, the converter is able to supply, theoretically, a 20% overload without falling into overmodulation. A normalized switching frequency (n) equal to 42 is chosen, based on practical considerations, such as switching losses. Thus, from (25), $X_C = 2.08$ pu, therefore, $C_o = 52\ \mu\text{F} \cong 50\ \mu\text{F}$ and, from (26), $i_{\text{dc, ref}} = 1.44$ pu $= 7.6$ A. On the other hand, the rectifier operates at the nominal delay angle (α) of 30° ($k_\alpha \cong 0.2$). Therefore, from (29) $L_{\text{dc}} = 25.6$ mH $\cong$ 25 mH.

V. Control Strategy Implementation Aspects

The control strategy is implemented on a three-phase 2-kVA laboratory prototype (Fig. 1) to verify its feasibility, to confirm the validity of the design procedure presented in Section IV, and to evaluate its static and transient performance. The front-end converter is a thyristor-based rectifier and the PWM CSI uses a diode-BJT combination as unidirectional power switches.

A digital system based on the TMS320C30 DSP board has been used to implement the control strategy. Fig. 4 shows the four main routines used to implement the rms load voltage reconstruction and control algorithms. *Routine A* runs on the host PC and allows the on-line communication with the DSP board through an user interface. Thus, the set points of the rms and frequency of the load voltage can be modified as well as monitored in real time. *Routines B, C,* and *D* run on the DSP board. Specifically, *Routine B* modifies and monitors the

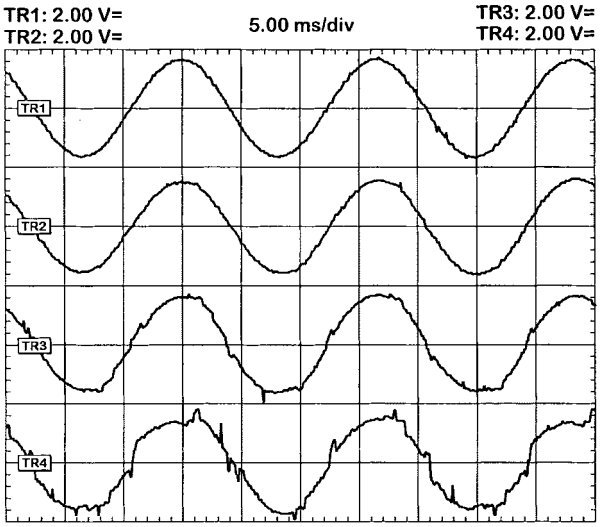


Fig. 5. Reconstructed line load voltage for different forgetting factors (λ). TR1: $\lambda = 1.00$. TR2: $\lambda = 0.97$. TR3: $\lambda = 0.90$. TR4: $\lambda = 0.80$. Experimental waveforms for $M_{\rm inv} = 0.95$, $i_{\rm dc} = 4$ A, $f_{sw} = 2.52$ kHz, and $f_o = 60$ Hz.

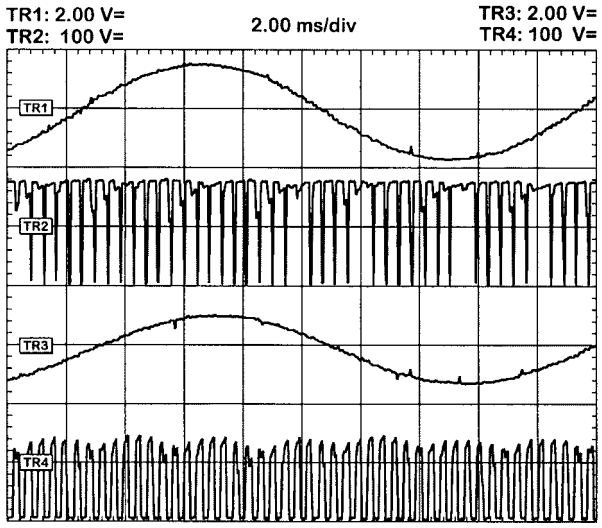


Fig. 6. Reconstructed load voltage and dc voltage for different CSI modulation indices ($M_{\rm inv}$). TR1: reconstructed load voltage ($\hat{v}_{ab}@M_{\rm inv} = 1$). TR2: dc voltage ($v_{\rm inv}@M_{\rm inv} = 1$). TR3: reconstructed load voltage ($\hat{v}_{ab}@M_{\rm inv} = 0.55$). TR4: dc voltage ($v_{\rm inv}@M_{\rm inv} = 0.55$). Experimental waveforms for $\lambda = 0.97$, $i_{\rm dc} = 4$ A, $f_{sw} = 2.52$ kHz, and $f_o = 60$ Hz.

rms and frequency of the load voltage, *Routine C* executes the reconstruction, control, and SVM algorithms, and *Routine D* sends the gating signals by means of the serial port of the microprocessor. Experimental tests showed that, with a minimum sample period of 120 μs, there is enough time to run the totality of routines required by the DSP system.

The gating signals are digitally generated using the SVM technique. This technique is preferred because of the straightforward implementation in digital systems. The SVM algorithm selects three switching combinations of the converter and their respective on times every sample time. The selection and on-time calculations are based upon the instantaneous modulation index ($M_{\rm inv}$) and sin and cos templates [Fig. 2(a)]. The switching combinations are then sequentially applied to the CSI [7]. The algorithm also generates and distributes the shorting pulses that are needed when zero line currents on the ac side of the CSI are required.

VI. Experimental Results

Many experimental tests have been performed to prove the feasibility of the control strategy based on the load voltage reconstruction algorithm. Steady-state tests to determine its accuracy and waveform quality are included (Figs. 5–11). Transient tests to demonstrate the tracking capabilities of the closed-loop control strategy are also presented (Figs. 12 and 13).

A. Voltage Reconstruction Algorithm Performance

The performance is investigated as a function of the forgetting factor (λ), the CSI modulation index ($M_{\rm inv}$), the ratio of the switching frequency (f_{sw}) to the load frequency (f_o), and load type.

1) The Forgetting Factor: (λ) defines the stability and tracking capabilities of the algorithm. The reconstructed load voltage waveforms for various values of λ are depicted in Fig. 5. Small values of λ (i.e., $\lambda = 0.80$) lead to numerical instabilities (Fig. 5, TR4), which are not present (Fig. 5, TR1) at high values of λ (i.e., $\lambda = 1.00$). However, to improve the tracking capabilities, a small value of λ is, indeed, required. From the experimental tests, a forgetting factor $\lambda = 0.97$ is selected.

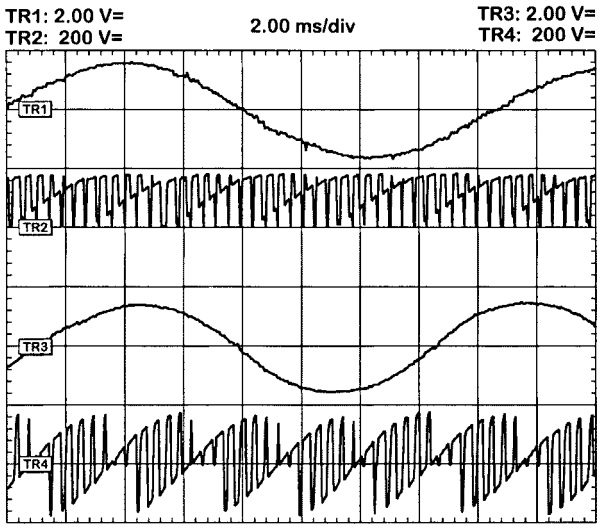


Fig. 7. Reconstructed load line voltage and dc voltage for resistive and no-load conditions. TR1: reconstructed load voltage ($\hat{v}_{ab}$, resistive load, $R = 33$ W). TR2: dc voltage ($v_{\rm inv}$, resistive load, $R = 33$ W). TR3: reconstructed load voltage ($\hat{v}_{ab}$, no-load). TR4: dc voltage ($v_{\rm inv}$, no-load). Experimental waveforms for $\lambda = 0.97$, $M_{\rm inv} = 0.95$, $i_{\rm dc} = 4$ A, $f_o = 60$ Hz, and $f_{sw} = 2.52$ kHz.

2) The CSI Modulation Index: ($M_{\rm inv}$) is used to control the load voltage while the dc-link current ($i_{\rm dc}$) is kept constant. Fig. 6 shows the reconstructed load ($\hat{v}_{ab}$) and CSI dc-link ($v_{\rm inv}$) voltages for two different modulation indices. For low modulation indices, the shorting pulses applied to the CSI become wider. Consequently, the CSI dc-link voltage presents

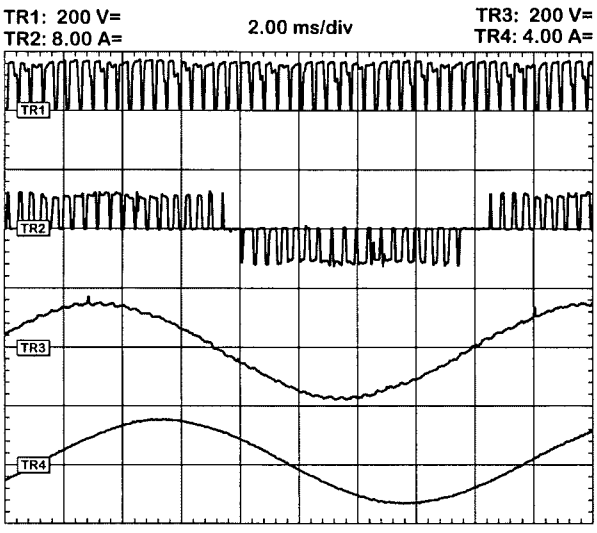


Fig. 8. Steady-state waveforms. TR1: dc voltage ($v_{\rm inv}$). TR2: CSI ac line current (i_{oa}). TR3: load line voltage (v_{ab}). TR4: load line current (i_a). Experimental waveforms for closed-loop operation and $\lambda = 0.97$, $v_{\rm rms,\,ref} = 120$ V, $i_{\rm dc} = 4$ A, $f_o = 60$ Hz, $f_{sw} = 2.52$ kHz, $R = 20\ \Omega$, and $L = 36$ mH.

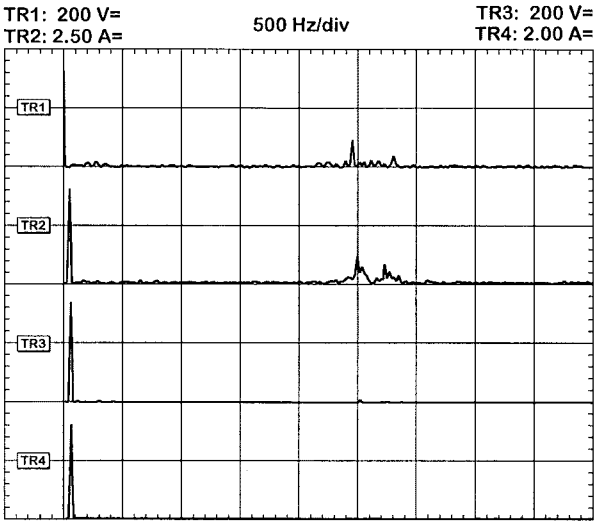


Fig. 9. Steady-state spectra. TR1: dc voltage ($v_{\rm inv}$). TR2: CSI ac line current (i_{oa}). TR3: load line voltage (v_{ab}). TR4: load line current (i_a). Experimental spectra for closed-loop operation and $\lambda = 0.97$, $v_{\rm rms,\,ref} = 120$ V, $i_{\rm dc} = 4$ A, $f_o = 60$ Hz, $f_{sw} = 2.52$ kHz, $R = 20\ \Omega$, and $L = 36$ mH.

wider zero voltage pulses (Fig. 6, TR4). Unfortunately, during zero dc voltage pulses, no information on the load voltages is available in the dc link. Therefore, at low modulation indices, low accuracy of the reconstructed load voltage is expected. In this paper, the deviation (Dev%) is defined as

$$\text{Dev}\% = \frac{\hat{v}_{\rm rms} - v_{\rm rms}}{v_{\rm rms}} \cdot 100. \tag{30}$$

Fig. 10 shows the deviation of the reconstructed rms load voltage versus the CSI modulation index for several operating points. For modulation indices smaller than 0.55, the deviation becomes larger than 5%, and it increases as $M_{\rm inv}$ decreases, as expected.

3) The Ratio fsw/f_o: The number of zero voltage pulses in the CSI dc-link voltage is proportional to the ratio f_{sw}/f_o.

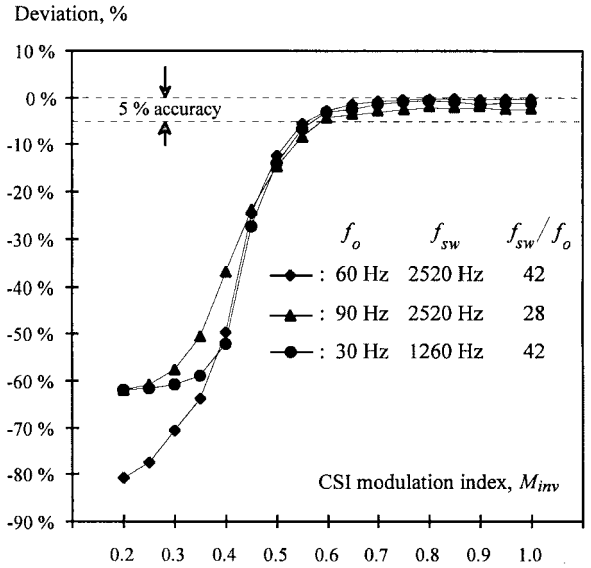


Fig. 10. Reconstructed rms load voltage ($\hat{v}_{\rm rms}$) accuracy as a function of the modulation index ($M_{\rm inv}$) for different load frequencies (f_o). Experimental results for $\lambda = 0.97$ and $i_{\rm dc} = 4$ A.

This ratio, therefore, affects the accuracy of the algorithm. In fact, this ratio should be kept constant to obtain constant accuracy. However, there is a maximum attainable switching frequency defined by the nature of the power switches and a minimum value required to avoid potential resonances between the load capacitive filter and the load itself. Fig. 10 includes the accuracy obtained for different f_{sw}/f_o ratios. As expected, when the ratio f_{sw}/f_o is constant (i.e., $f_{sw}/f_o = 2.52$ kHz/60 Hz $= 1.26$ kHz/30 Hz $= 42$), the accuracy is approximately constant (for modulation indices higher than 0.55). On the contrary, for lower ratios of f_{sw}/f_o (i.e., $f_{sw}/f_o = 2.52$ kHz/90 Hz $= 28$), the accuracy is deteriorated. Note that if the switching frequency is kept constant, the accuracy increases as the output frequency decreases.

4) The Load Type: Fig. 7 shows the reconstructed load and CSI dc-link voltage waveforms for a resistive load and at no load. Experimental tests demonstrate that accuracy is not dependent on load type. This results from the fact that the information available in the dc-link voltage (Fig. 7, TR2 and TR4) remains approximately constant, regardless of the load type.

B. Static and Transient Performance

1) Steady-State Performance: Key experimental waveforms are shown in Fig. 8 for a steady-state operating condition. Fig. 9 shows the corresponding spectra. Also, Fig. 11 shows the load voltage harmonic distortion (THD) for $S_{\rm load} = 750$ VA and for no-load conditions as a function of the load rms voltage. The THD is defined as

$$\text{THD}\% = \frac{100}{v_{\rm rms,\,1}} \sqrt{\sum_{h=2}^{\infty} v_{{\rm rms},\,h}^2}. \tag{31}$$

From the experimental results, it can be observed that: 1) the line current (Fig. 8, TR2) is of the PWM type and, thereby, the harmonic components are at the switching frequency and

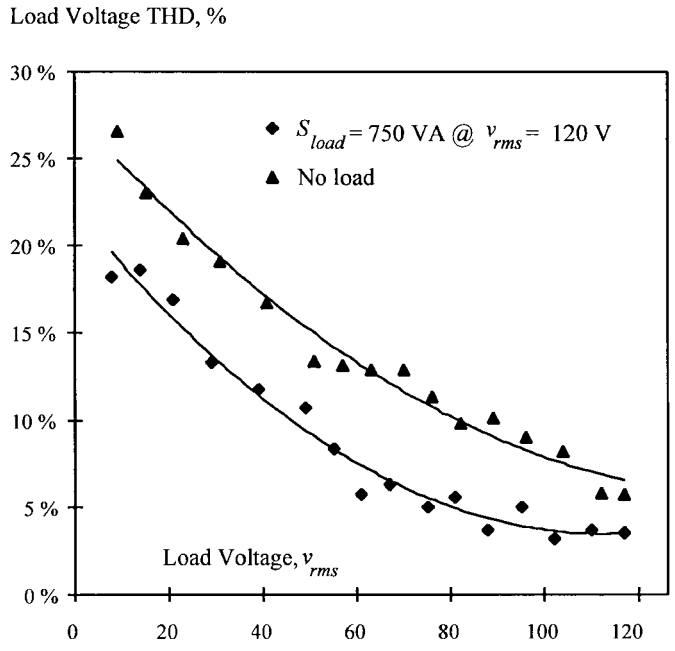


Fig. 11. Load voltage THD as a function of the load rms voltage ($v_{\rm rms}$). Experimental results for closed loop and $\lambda = 0.97$, $i_{\rm dc} = 4$ A, $f_o = 60$ Hz, and $f_{sw} = 2.52$ kHz.

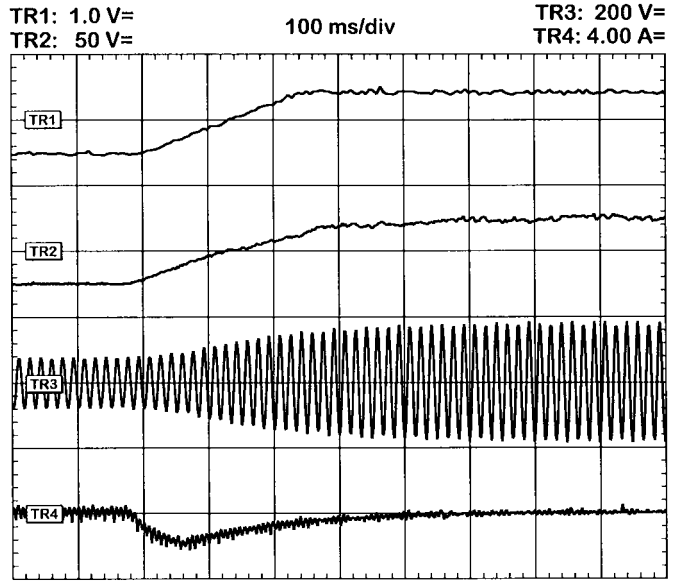


Fig. 12. Load voltage reference ramp-up. TR1: load rms voltage reference ($v_{\rm rms,ref}$). TR2: load rms voltage ($\hat{v}_{\rm rms}$). TR3: load line voltage (v_{ab}). TR4: dc-link current ($i_{\rm dc}$). Experimental transient response for $\lambda = 0.97$, $v_{\rm rms,ref} = 70 \rightarrow 120$ V, $i_{\rm dc} = 4$ A, $f_o = 60$ Hz, and $f_{sw} = 2.52$ kHz.

multiples (Fig. 9, TR2); 2) the current harmonics feature amplitudes lower than the fundamental component which validates the design guidelines of the load filter (Fig. 9, TR2); 3) the load voltage (Fig. 8, TR3) has very low ripple due to the PWM nature of the line current and proper filtering action of the capacitive filter (THD% $= 3.5\%$ @ $S_{\rm load} = 750$ VA and $v_{\rm rms} = 117$, Fig. 11); 4) there is an increase in the THD at low load voltages due to the lower modulation index required to control the voltage (Fig. 11); and 5) the harmonic distortion

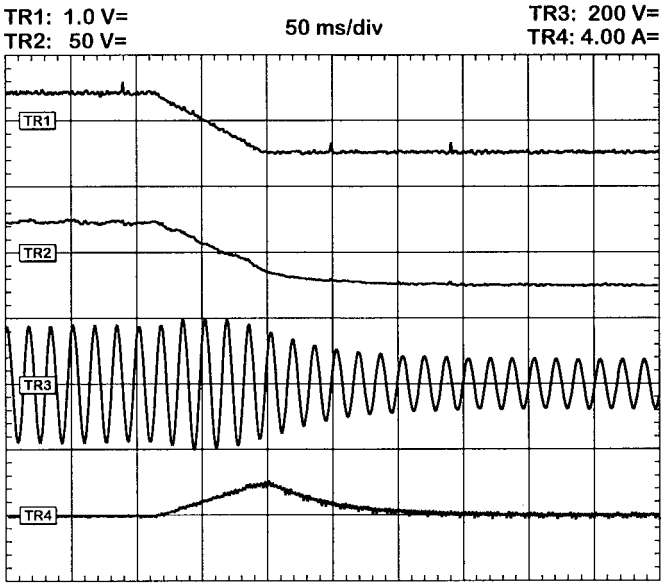


Fig. 13. Load voltage reference ramp-down. TR1: load rms voltage reference ($v_{\rm rms,ref}$). TR2: load rms voltage ($\hat{v}_{\rm rms}$). TR3: load line voltage (v_{ab}). TR4: dc-link current ($i_{\rm dc}$). Experimental transient response for $\lambda = 0.97$, $v_{\rm rms,ref} = 120 \rightarrow 70$ V, $i_{\rm dc} = 4$ A, $f_o = 60$ Hz, and $f_{sw} = 2.52$ kHz.

increases under no-load conditions as the filter absorbs the total harmonic content of the PWM current (Fig. 11).

2) Transient Performance: Transient waveforms of the closed-loop operation are depicted in Figs. 12 and 13. The rms load voltage reference describes a ramp-up (Fig. 12, TR1) and ramp-down (Fig. 13, TR1) trajectory, respectively. It can be seen that: 1) in both cases, the actual rms load voltage tracks the references (Fig. 12, TR2 and Fig. 13, TR2); 2) the steady-state error is minimized by the integration action of the rms load voltage controller; and 3) the dc-link current presents an undershoot (Fig. 12, TR4) and an overshoot (Fig. 13, TR4), respectively, during transient conditions. These are corrected by the independent dc-bus current controller.

VII. Conclusions

This paper has demonstrated the feasibility of a DSP-based load voltage control scheme for a CSI suitable for a general power supply. The transducer count is reduced and ruggedness therefore increases. The load voltage estimation is based on load ac voltage reconstruction by means of an RLSE algorithm which uses the information available on the dc-bus voltage and acknowledgement of the CSI switching information. Experimental results show that the algorithm features an error of at most 4% for modulation indices higher than 0.55. The gating pattern is generated by an SVM that provides low load voltage harmonic distortion. In fact, at nominal load voltage and under worst case conditions (no load), a distortion of 5% is obtained. The short execution time (of the order of 120 μs) of the DSP algorithms allows switching frequencies up to 8.3 kHz, which falls in the range of typical medium-power converters. This paper includes the experimental results that demonstrate the feasibility, accuracy, and tracking capabilities of the algorithm. The data are obtained on a three-phase 2-kVA CSI laboratory prototype.

APPENDIX A
NONRECURSIVE LSE

The scalar $J_i(i = 1, 2, 3)$ is defined as the accumulated square error after N weighted samples as

$$J_i = \sum_{t_k=t_1}^{t_N} w(t_k)(y_i(t_k) - \hat{y}_i(t_k))^2 \tag{A1}$$

where $w(t_k)$ is the weighting coefficient $(0 \le w(t_k) \le 1)$. Equation (A1) can be written as

$$J_i = \{\mathbf{Y}_i(t_N) - \hat{\mathbf{Y}}_i(t_N)\}^T \mathbf{W}(t_N)\{\mathbf{Y}_i(t_N) - \hat{\mathbf{Y}}_i(t_N)\}. \tag{A2}$$

Considering that $\hat{\mathbf{Y}}_i(t_N) = \mathbf{M}(t_N)\hat{\theta}_i(t_N)$, (A2) yields

$$\begin{aligned} J_i = {} & \mathbf{Y}_i^T(t_N)\mathbf{W}(t_N)\mathbf{Y}_i(t_N) - 2\hat{\theta}_i^T(t_N)\mathbf{M}^T(t_N)\mathbf{W}(t_N) \\ & \times \mathbf{Y}_i(t_N) + \hat{\theta}_i^T(t_N)\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N)\hat{\theta}_i(t_N). \end{aligned} \tag{A3}$$

In order to minimize the error J_i, (A3) is differentiated with respect to $\hat{\theta}_i$, which gives

$$\begin{aligned} \frac{\partial J_i}{\partial \hat{\theta}_i(t_N)} = {} & -2\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{Y}_i(t_N) \\ & + 2\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N)\hat{\theta}_i(t_N) \end{aligned} \tag{A4}$$

and to obtain the coefficients that minimize J_i, (A4) is equated to zero, which yields

$$\begin{aligned} \hat{\theta}_i(t_N) = {} & \{\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N)\}^{-1} \\ & \times \mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{Y}_i(t_N). \end{aligned} \tag{A5}$$

In order to prove that the above solution represents a minimum, the second differential of J_i is analyzed. From (A4), we obtain

$$\frac{\partial^2 J_i}{\partial^2 \hat{\theta}_i(t_N)} = 2\mathbf{M}^T(t_N)\mathbf{W}(t_N)\mathbf{M}(t_N). \tag{A6}$$

Since $w(t_k)$ are all positive, $M^T(t_N)W(t_N)M(t_N)$ is semidefined positive [13] and, therefore, (A5) is the solution that minimizes J_i.

APPENDIX B
PROPAGATION MATRIX CALCULATION

The propagation matrix $\mathbf{P}(t_N)$ satisfies

$$\mathbf{P}^{-1}(t_N) = \lambda\mathbf{P}^{-1}(t_{N-1}) + \mathbf{N}(t_N)\mathbf{N}^T(t_N). \tag{A7}$$

Premultiplying (A7) by $\mathbf{P}(t_N)$ and then postmultiplying by $\mathbf{P}(t_{N-1})\mathbf{N}(t_N)$, we obtain

$$\frac{\mathbf{P}(t_{N-1})\mathbf{N}(t_N)}{\lambda + \mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})\mathbf{N}(t_N)} = \mathbf{P}(t_N)\mathbf{N}(t_N). \tag{A8}$$

Postmultiplying (A8) by $\mathbf{N}^T(t_N)$ and using (A7) yields

$$\frac{P(t_{N-1})\mathbf{N}(t_N)\mathbf{N}^T(t_N)}{\lambda + \mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})\mathbf{N}(t_N)} = \mathbf{I} - \lambda\mathbf{P}(t_N)\mathbf{P}^{-1}(t_{N-1}). \tag{A9}$$

Finally, postmultiplying (A9) by $\mathbf{P}(t_{N-1})$ and reorganizing terms, we obtain

$$\begin{aligned} & \mathbf{P}(t_N) \\ & = \frac{1}{\lambda}\left\{\mathbf{P}(t_{N-1}) - \frac{\mathbf{P}(t_{N-1})\mathbf{N}(t_N)\mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})}{\lambda + \mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})\mathbf{N}(t_N)}\right\}. \end{aligned} \tag{A10}$$

Note that the factor $\lambda + \mathbf{N}^T(t_N)\mathbf{P}(t_{N-1})\mathbf{N}(t_N)$ in (A10) is a scalar. Therefore, (A10) allows us to calculate recursively the propagation matrix $\mathbf{P}(t_N)$ without requiring a matrix inversion.

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REFERENCES

[1] B. Bose, "Recent advances in power electronics," *IEEE Trans. Power Electron.*, vol. 7, pp. 2–16, Jan. 1992.
[2] E. Wiechmann, P. Ziogas, and V. Stefanovic, "A novel bilateral power conversion scheme for variable frequency static power supplies," *IEEE Trans. Ind. Applicat.*, vol. IA-21, pp. 1126–1233, Sept./Oct. 1985.
[3] H. Karshenas, H. Kojori, and S. Dewan, "Generalized techniques of selective harmonic elimination and current control in current source inverters/converters," *IEEE Trans. Power Electron.*, vol. 10, pp. 566–573, Sept. 1995.
[4] P. Enjeti, P. Ziogas, and J. Lindsay, "A current source PWM inverter with instantaneous current control capability," *IEEE Trans. Ind. Applicat.*, vol. 27, pp. 893–643, May/June 1991.
[5] S. Nonaka and Y. Neba, "A PWM GTO current source converter–inverter system with sinusoidal inputs and outputs," *IEEE Trans. Ind. Applicat.*, vol. 25, pp. 76–85, Jan./Feb. 1989.
[6] G. Joós, G. Moschopoulos, and P. Ziogas, "A high performance current source inverter," in *Conf. Rec. IEEE PESC'91*, June 1991, pp. 123–130.
[7] J. Espinoza and G. Joós, "Current source converter on-line pattern generator switching frequency minimization," *IEEE Trans. Ind. Electron.*, vol. 44, pp. 198–206, Apr. 1997.
[8] J. Holtz, "Pulsewidth modulation—A survey," *IEEE Trans. Ind. Electron.*, vol. 39, pp. 410–420, Oct. 1992.
[9] J. Espinoza, G. Joós, and P. Ziogas, "Voltage controlled current source inverters," in *Conf. Rec. IEEE IECON'92*, Nov. 1992, pp. 512–517.
[10] Y. Nishida and T. Haneyoshi, "Predictive Instantaneous value controlled PWM inverter for UPS," in *Conf. Rec. IEEE PESC'92*, June/July 1992, pp. 776–783.
[11] T. Green and B. Williams, "Derivation of motor line-current waveforms from the dc link current of an inverter," *Proc. Inst. Elect. Eng.*, vol. 136, pt. B, no. 4, pp. 196–204, July 1989.
[12] F. Petruzziello, G. Joós, and P. Ziogas, "Some implementation aspects of line current reconstruction in three phase PWM inverters," in *Conf. Rec. IEEE IECON'90*, Nov. 1990, pp. 1149–1154.
[13] N. Sinha, *Modeling and Identification of Dynamic Systems.* New York: Van Nostrand Reinhold, 1983.

José R. Espinoza (S'93–M'98), for a photograph and biography, see p. 87 of the February 1998 issue of this TRANSACTIONS.

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