# Performance of a Single-Stage UPS System for Single-Phase Trapezoidal-Shaped AC-Voltage Supplies

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***Abstract*— A high-performance single-stage UPS system for single-phase ac power supply systems is presented. The topology generates a trapezoidal-shaped load voltage that is synchronized with the ac supply, therefore, a small dc-link capacitor is required. This feature leads to a high-input power factor (0.94 at nominal voltage), and due to the single-stage structure, high efficiency (93% at nominal voltage) is also achieved. Moreover, in both cases the supply current spectrum presents low-order harmonics, all of which satisfy IEC 555. The high performance is validated using both resistive (linear) and diode $RC$ (nonlinear) loads. The dynamic performance of the UPS system is also analyzed under different transient conditions. Specifically, the supply to battery, battery to supply transition, load transient, and supply/battery-voltage transients are performed. They show a transfer time of 500 $\mu$s (from ac supply to battery) and overvoltages of at most 15%. The dynamic and static evaluations are performed on a 1-kVA UPS system. The design guidelines for the key components and control parameters are also included.**

***Index Terms*— AC mains synchronization, PWM inverter, single-phase single-stage conversion topology, trapezoidal-shaped ac output voltage, UPS.**

## I. Introduction

IN THE conversing CATV and telecommunication market, the hybrid fiber/coax networks are becoming very attractive [1]–[3]. These networks require single-phase ac power supplies that deliver trapezoidal-shaped voltage waveforms [4]. Additional requirements are high-input power factor, high overall efficiency, and increased reliability. Since the continuity of the power distribution system is not totally guaranteed, UPS systems that satisfy the above constraints are required [5], [6].

In conventional UPS systems, high power factor is achieved by employing an additional power-factor-correction (PFC) stage [Fig. 1(a)] [7]. Unfortunately, this additional stage limits the overall efficiency and reduces reliability. In this work, to achieve high-input power factor and high overall efficiency while providing high-quality trapezoidal-shaped load voltage, a single-stage UPS system is proposed [Fig. 1(b)].

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The basic power structure was introduced in [8]. The main feature of the UPS is a load voltage synchronized with the ac supply, and, therefore, a small dc-link capacitor is required (Fig. 2). The above feature leads to the following improvements: 1) the input current is in phase with the ac supply voltage (unity displacement factor is achieved) and 2) the input current presents a low-harmonic distortion that satisfies the IEC 555 requirements, including nonlinear loads. Both features result in a high overall input power factor (0.94). In addition, since the scheme is implemented in a single stage, high overall efficiency (93%) and high reliability are also achieved.

This paper presents the steady-state and transient performance of the proposed UPS system under different conditions. The input power factor and efficiency as a function of the load level and supply voltage are included. Transient tests such are: 1) supply–battery transition; 2) battery–supply transition; 3) load transients; and 4) supply/battery-voltage transients are also included. A small-signal model of the UPS system is derived to analyze and generalize the experimental transient results. Design guidelines for the key components and controller parameters are also included. Experimental results are obtained on a 1-kVA UPS system.

## II. UPS System Description

### A. Power Topology

As stated in the introduction, optical fiber/coax cable hybrid networks require single-phase ac power supplies that generate a trapezoidal-shaped voltage waveform. Therefore, off-line UPS systems are not applicable [9]. Instead, a standby structure based on a single conversion stage is proposed [Fig. 1(b)]. Additional specifications of the system are presented in Table I.

A detailed diagram of the power topology is depicted in Fig. 2. The main components of the system are the diode rectifier, pulsewidth modulation (PWM) inverter, input/output filter, dc-link capacitor, battery charger and battery, battery on/off switch, and load transformer. The topology can operate in two different modes, namely, *normal/charging* and *backup* modes. In the *normal/charging* mode, the battery on/off switch is opened. Therefore, the ac mains supplies the load power throughout the PWM inverter and charges the battery at constant current as well. In the *backup* mode, the ac mains is not available and the battery on/off switch is closed.

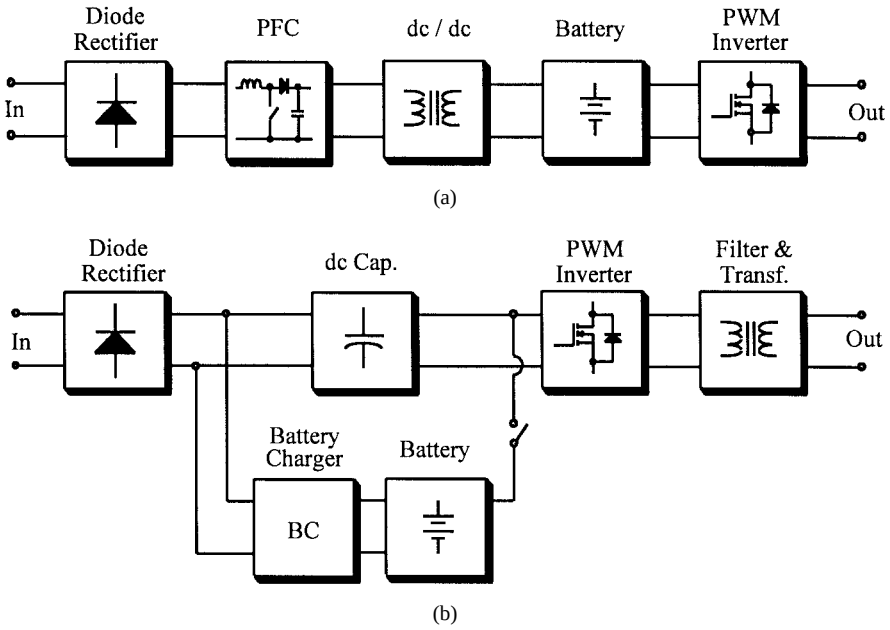


Fig. 1. High-performance UPS topologies for single-phase power supply systems: (a) conventional approach and (b) proposed scheme.

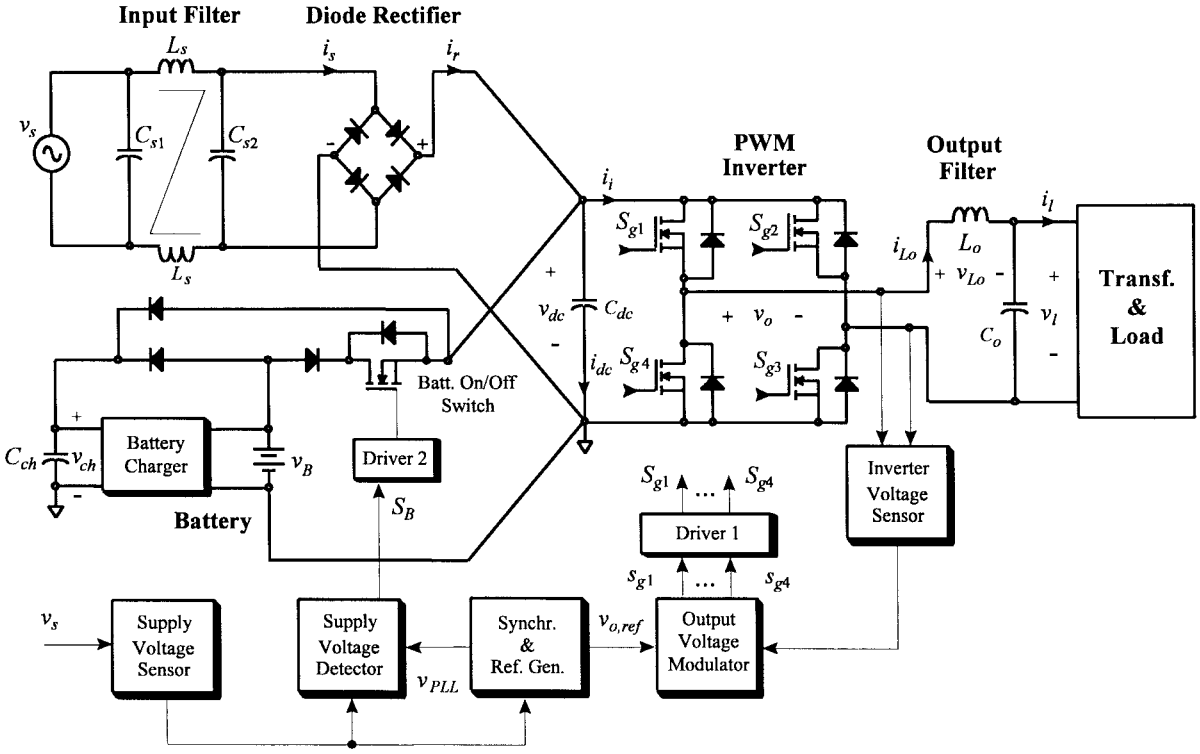


Fig. 2. Proposed UPS power circuit configuration and control strategy.

Thus, the battery supplies the load power. Fig. 3 shows the ideal steady-state waveforms in the normal/charging operating mode for a resistive load. In Fig. 3, and in order to clearly show the operating principles, a low-switching frequency ($f_{sw} = 44$ p.u.) has been used and the current drawn by the battery charger has been neglected. A brief description of the components of the power topology and waveforms is as follows.

The **diode rectifier** is a single-phase full-wave rectifier and provides a dc voltage across the dc-link capacitor [$v_{\rm dc}$, Fig. 3(b)]. The **PWM inverter** is a single-phase full-wave converter, where MOSFET's are used as power switches, which are modulated using a carrier-based PWM technique. In the actual implementation, a 40-kHz switching frequency ($f_{sw} = 40$ kHz) was used. The output voltage is a PWM waveform [$v_o$, Fig. 3(d)] that is synchronized with the ac mains.

TABLE I
IUPS SYSTEM SPECIFICATIONS

| Specification | Parameter | Value |
|---|---|---|
| **ac Input** | voltage | 115 V ± 20 %, 1ϕ |
| | frequency | 60 Hz ± 3 Hz |
| **ac Output** | voltage | 90 V ± 3 V, Trapezoidal |
| | frequency | 60 Hz ± 3 Hz |
| | rising edge slew rate | 100 ± 50 mV/μ s |
| | falling edge slew rate | 100 ± 50 mV/μ s |
| **Transfer Time** | ac supply to battery | 8.3 ms |
| | battery to ac supply | < 100 ms |
| **Overall Performance** | input power factor | > 0.9 |
| | efficiency | > 85 % |

The appropriate gating signals are generated by the *output-voltage modulator* (Fig. 2). The **input filter** ($L_s$, $C_{s1}$, $C_{s2}$) is basically an electromagnetic interference (EMI) filter, and, thereby, it does not affect the 60-Hz current component. The **output filter** ($L_o$, $C_o$) filters out the high-frequency-voltage components generated by the PWM operation of the inverter and defines the trapezoidal-shaped load voltage [$v_l$, Fig. 3(e)]. Since the output voltage [$v_o$, Fig. 3(d)] is forced to be in phase with the ac mains, the function of the **dc-link capacitor** ($C_{\rm dc}$) is only to filter out the current harmonics generated by the PWM operation of the inverter. Thus, small values of $C_{\rm dc}$ provide enough filtering action while providing high-input power factor [8]. Section III provides design guidelines for the output filter ($L_o$, $C_o$) and dc-link capacitor ($C_{\rm dc}$).

The **battery charger** is a standard forward dc/dc converter with five secondaries [(Fig. 4) 100 W maximum, 50 W nominal]. The dc-input voltage is supplied by the capacitor $C_{ch}$ (Fig. 2), and, thereby, it should ensure a minimum dc voltage. Section III provides design guidelines for $C_{ch}$. The main channel charges the battery, and the other four channels are used to generate regulated dc voltages to power up the logic, drivers, and protections. The control of the main channel is carried out by means of the UC 2845 IC, which allows peak current mode control and voltage regulation as well. The current mode control allows both current limiting and constant charging current capabilities [7]. The **battery on/off switch** is actually an MOSFET switch that allows the transition between the *normal/charging* and *backup* mode and vice versa. The switch is commanded from the *supply-voltage detector block* (Fig. 2). Finally, the **load transformer** isolates and steps-up the load voltage. The transformer operates at 60 Hz and features a 1 : 1.5 turns ratio.

One problem associated with the battery-charge/discharge circuit is that the storage batteries are directly connected to ac mains. Therefore, all wiring and electrical connections to and between the batteries require the enhanced insulation to satisfy the safety regulatory requirements as per UL, IEC, and CSA. Additional circuitry for protection against accidental contact with the batteries posts also would need to be provided. However, in many current hybrid fiber/coax architectures, where the isolated ac is provided, this is not a limitation.

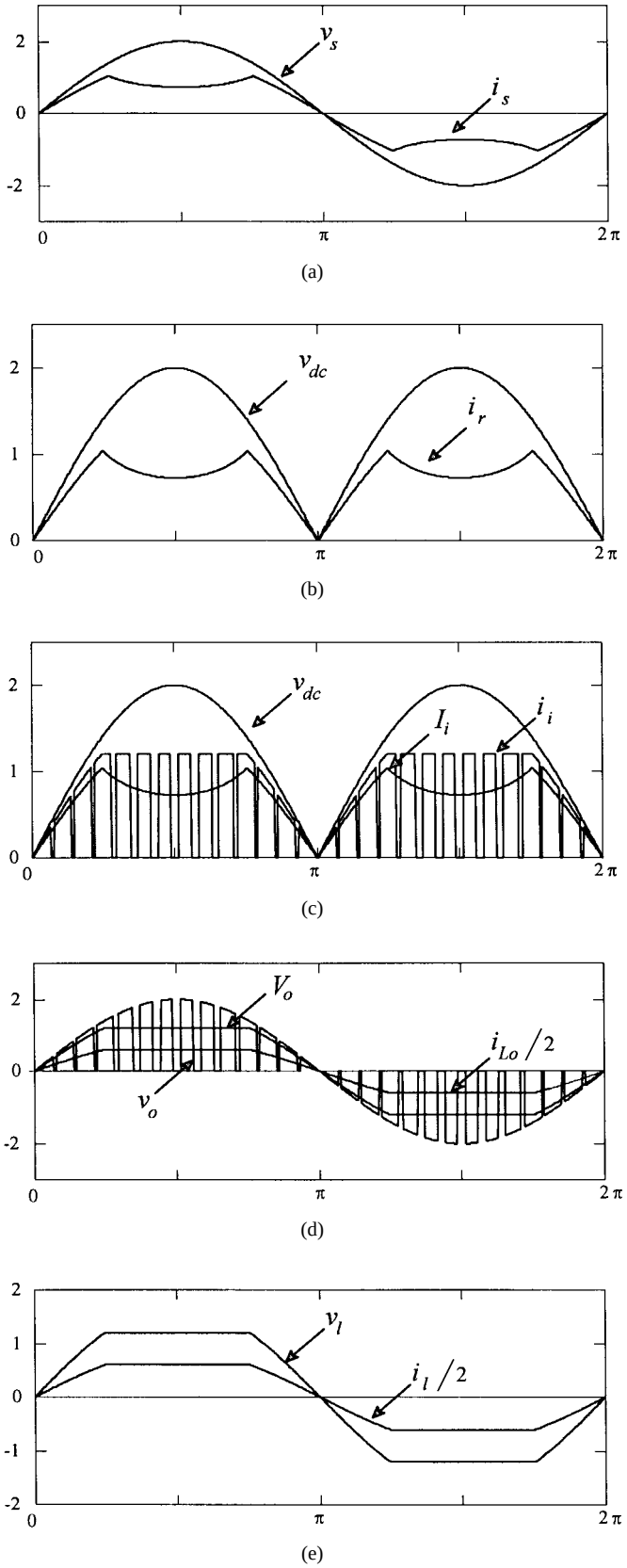


Fig. 3. Normalized steady-state waveforms of the power circuit in the *normal/charging* operating mode (simulated results for $f_{sw} = 44$ p.u.). (a) Supply voltage ($v_s$) and supply current ($i_s$), (b) dc-link voltage ($v_{\rm dc}$) and rectifier dc current ($i_r$), (c) dc-link voltage ($v_{\rm dc}$), inverter dc current ($i_i$), and inverter averaged dc current ($I_i$), (d) inverter ac voltage ($v_o$), inverter averaged ac voltage ($V_o$), and inductor current ($v_{L_o}$), and (e) load voltage ($v_l$) and current ($i_l$).

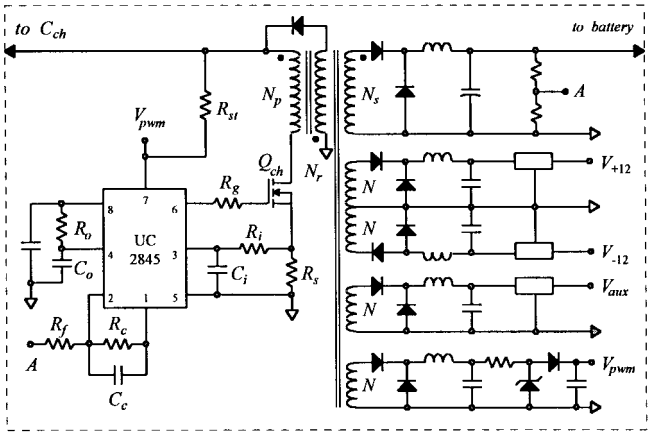


Fig. 4. Battery-charger circuit realization.

### B. Control Strategy

The control strategy is primarily based on two control loops (Fig. 2): the load voltage and the battery switch on/off loops. The load-voltage loop is a feedback strategy that forces the inverter averaged output voltage ($V_o$, Fig. 3) to be equal to the voltage reference ($v_{o,\mathrm{ref}}$). Due to the high-switching frequency of the PWM inverter (40 kHz), a high bandwidth (20 kHz in this design) can be obtained, and thereby high-load-voltage quality can be achieved even under transient conditions. Fig. 5(a) shows the *output-voltage modulator* scheme that performs the load-voltage regulation. Fig. 6 shows the relevant waveforms of the *output-voltage modulator*, where a low-switching frequency ($f_{sw} = 44$ p.u.) has been used to clearly show the operating principle. The scheme integrates the error and then compares the resulting signal ($m$, Fig. 6) with an internal triangular carrier ($v_{tri}$, Fig. 6). The triangular carrier frequency is 40 kHz, and the integrator time constant is chosen the smallest possible to ensure a wide bandwidth. Section III provides design guidelines for the integrator time constant ($T_i$). The gating patterns $s_{g1}$, $s_{g2}$, $s_{g3}$, and $s_{g4}$ are amplified by the *driver 1 block* (Fig. 2), which finally generates the gating signals $S_{g1}$, $S_{g2}$, $S_{g3}$, and $S_{g4}$. The *driver 1 block* consists of two drivers of type IR 2110.

The load-voltage reference ($v_{o,\mathrm{ref}}$) is generated by the *synchronization and reference generator block* (Fig. 2), which is basically a phase-locked loop (PLL) circuit synchronized with the ac supply voltage. An alternative realization of this block is presented in Fig. 5(b). The sensed supply voltage ($v_s$) feeds a PLL (based on the LM 565 chip) and thereby a sinusoidal signal synchronized with the ac mains is generated ($v_{\mathrm{PLL}}$). A limiting circuit is used to finally provide a trapezoidal-shaped reference ($v_{o,\mathrm{ref}}$). Under complete absence of the ac supply, the PLL holds the signal $v_{\mathrm{PLL}}$ at 60 Hz in a free-running mode. Once the ac mains is reestablished, the PLL requires some time (approximately 20 ms in this application) to synchronize back the signal $v_{\mathrm{PLL}}$ with the supply voltage.

The second control loop is the battery switch on/off (Fig. 2). This loop is implemented by the *supply-voltage detector block* and basically provides the signal $S_B$ to the battery on/off switch. As soon as the ac supply fails, the signal $S_B$ goes on and the battery takes over, providing the load power. When the ac supply comes back, the signal $S_B$ remains on for sometime (60 ms in this design) allowing the PLL circuit to synchronize back with the ac supply voltage. In this work, the block diagram depicted in Fig. 5(c) was implemented as the *supply-voltage detector*. The actual sensed supply voltage ($v_s$) and the PLL output signal ($v_{\mathrm{PLL}}$) are compared on a continuous basis, and the signal $S_{a/c}$ is thus generated. The internal *falling-edge delay block* ensures that the battery is switched off only after the load-voltage reference is synchronized with the ac mains. The final *isolation block* is required due to the actual location of the battery on/off switch.

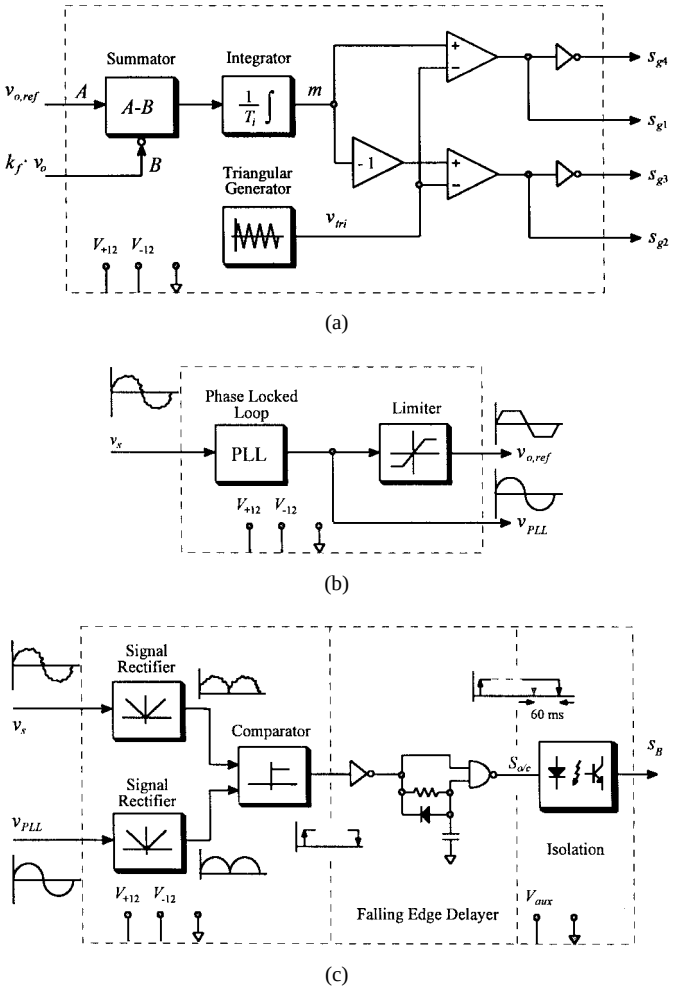


Fig. 5. Control blocks: (a) output-voltage modulator, (b) synchronization and reference generator, and (c) supply-voltage detector.

## III. Design Guidelines

This section presents the design guidelines for the key components of the UPS system. Specifically, the design of the dc-link capacitor ($C_{\mathrm{dc}}$), the second-order output filter ($L_o$, $C_o$), the battery-charger input capacitor ($C_{ch}$), and the integrator time constant ($T_i$) are addressed.

### A. The DC-Link Capacitor ($C_{\mathrm{dc}}$)

It has been reported that small values of $C_{\mathrm{dc}}$ lead to reduced input-current distortion and high-input power factor [8]. However, the dc-link capacitor has to be large enough to

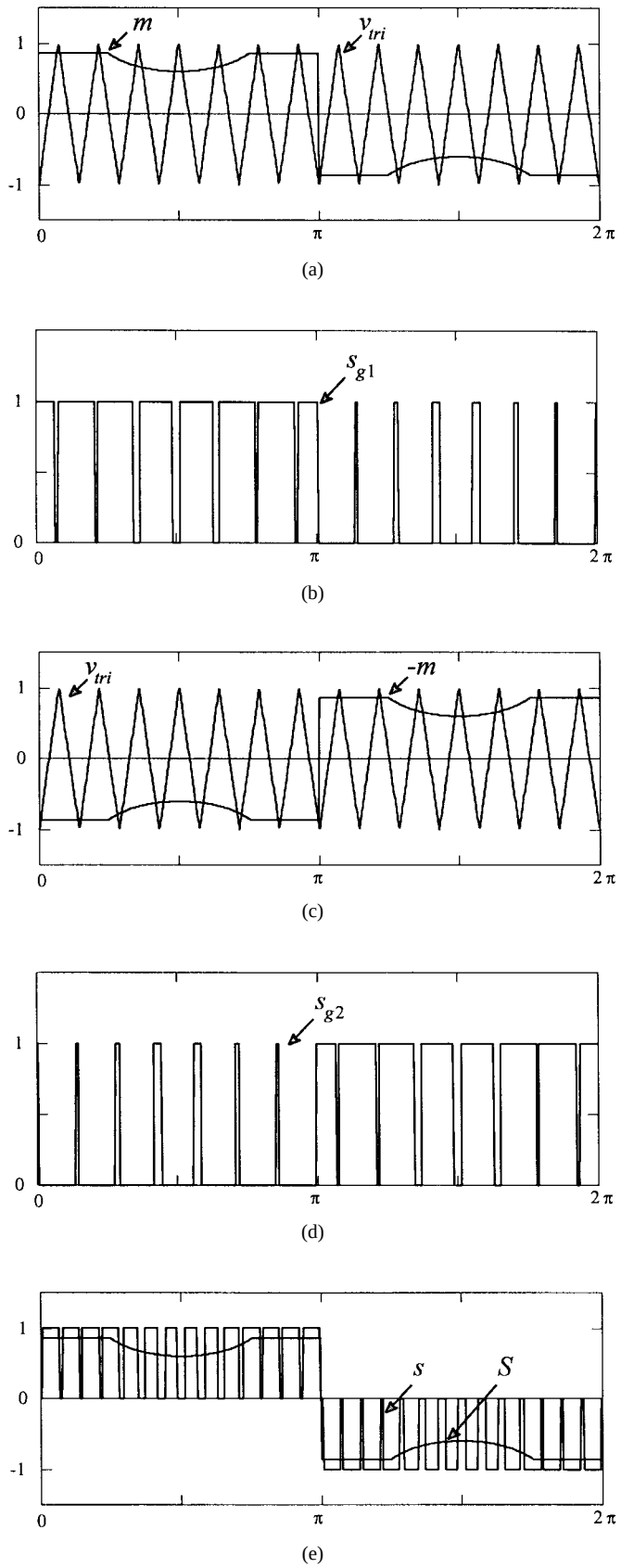


Fig. 6. Normalized steady-state waveforms of the output-voltage modulator (simulated results for $f_{sw} = 44$ p.u.). (a) Triangular carrier ($v_{tri}$) and modulating waveform ($m$), (b) gating signal, switch 1 ($sg_1$), (c) triangular carrier ($v_{tri}$) and inverted modulating waveform ($-m$), (d) gating signal, switch 2 ($sg_2$), and (e) switching function ($s$) and averaged switching function ($S$).

filter out the high-frequency current harmonics generated by the PWM operation of the inverter [see $i_i$ in Fig. 3(c)]. This work proposes to design $C_{\rm dc}$ by limiting the maximum dc-link peak-to-peak voltage ripple in one switching period to a given value $\Delta v_{\rm dc}$. Thus, the dc-link voltage keeps the original full-wave rectified voltage waveform, where the high-frequency harmonics are limited to $\Delta v_{\rm dc}$.

For designing purposes, the worst case is to assume that all current harmonics contained in the inverter ac current [$i_i$ in Fig. 3(c)] are absorbed by the dc-link capacitor. Fig. 7 shows the resulting current ($i_{\rm dc}$) which would flow through the capacitor in this case. This waveform is obtained by subtracting the inverter ac current [$i_i$ in Fig. 3(c)] from the rectifier dc current [$i_r$ in Fig. 3(b)]. This PWM current generates in each switching period a triangular voltage ripple ($\Delta v_{\rm dc}$) across the dc-link capacitor. Noting that the peak-to-peak current that flows through the capacitor in each switching period is $i_{L_o}$, the amplitude of the peak-to-peak voltage ripple $\Delta v_{\rm dc}$ can be written as

$$\Delta v_{\rm dc} = \frac{1}{C_{\rm dc}}\, i_{L_o}\, \frac{S}{2f_{sw}} \tag{1}$$

where $S$ is the averaged switching function [Fig. 6(e)] which is obtained from the desired load voltage ($v_l$) and available dc-link voltage ($v_{\rm dc}$) as

$$0 < S = \frac{v_l}{v_{\rm dc}} < 1. \tag{2}$$

If the second-order load filter generates a load voltage with reduced harmonic distortion, the inductor current ($i_{L_o}$) can be considered equal to the load current ($i_l$). Thus

$$i_{L_o} = \frac{v_l}{R_l}. \tag{3}$$

By combining (1)–(3) the normalized peak-to-peak dc-link voltage ripple can be expressed as

$$\frac{\Delta v_{\rm dc}}{v_{\rm dc}} = \frac{X_{C_{\rm dc}}\pi}{f_{sw}} S^2 \tag{4}$$

where $X_{C_{\rm dc}}$ is the normalized dc-link capacitor impedance and $f_{sw}$ is the normalized switching frequency. The normalized peak-to-peak dc-link voltage ripple (4) is a function of the averaged switching function $S$. However, the maximum value of $S$ is one, therefore, the maximum capacitor impedance for a given maximum normalized voltage ripple can be written as

$$X_{C_{\rm dc},\max} = \frac{f_{sw}}{\pi} \left(\frac{\Delta v_{\rm dc}}{v_{\rm dc}}\right)_{\max}. \tag{5}$$

### *B. The Load Second-Order Filter ($L_o$, $C_o$)*

The load filter should be small enough to minimize the phase shift between the load current ($i_l$) and the inverter ac voltage ($v_o$). This come from the fact that any phase shift will be reflected back as an input displacement power factor, which, in turn, will deteriorate the overall input power factor. However, the load filter should be large enough to define a trapezoidal-shaped load-voltage waveform with reduced harmonic components. In this paper, the inductor ($L_o$) is designed

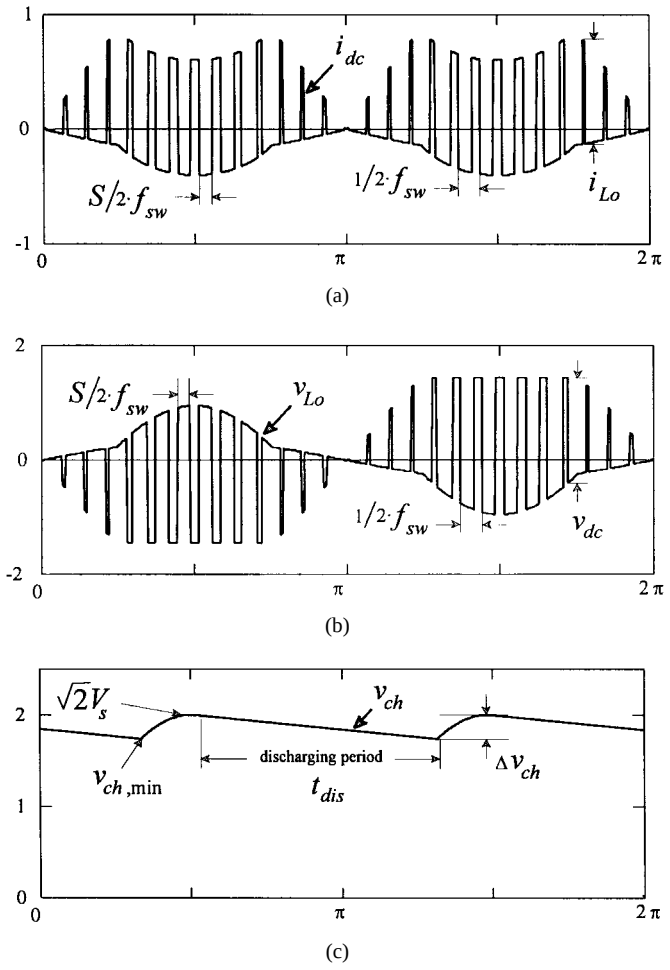


Fig. 7. Normalized steady-state waveforms of the power circuit for design purposes (simulated results for $f_{sw} = 44$ p.u.). (a) DC-link capacitor current ($i_{\rm dc}$), (b) load filter inductor voltage ($v_{L_o}$), and (c) battery-charger dc-supply voltage ($v_{ch}$).

to operate in continuous mode, and the capacitor ($C_o$) to limit the maximum load-voltage ripple.

1) ***The inductor $L_o$*** has between its terminals a voltage ($v_{L_o}$) as shown in Fig. 7(b). The inductor voltage is obtained by subtracting the load voltage ($v_l$) from the inverter ac voltage ($v_o$). Thus, the peak-to-peak voltage across the inductor $L_o$ is the dc-link voltage ($v_{\rm dc}$) in each switching period [Fig. 7(b)]. Therefore, the peak-to-peak current ripple ($\Delta i_{L_o}$) in $L_o$ can be written as

$$\Delta i_{L_o} = \frac{1}{L_o}\, v_{\rm dc}\, \frac{S}{2 f_{sw}}. \tag{6}$$

By combining (2), (3), and (6), the normalized peak-to-peak inductor current can be expressed as

$$\frac{\Delta i_{L_o}}{i_{L_o}} = \frac{\pi}{X_{L_o} f_{sw}} \tag{7}$$

where $X_{L_o}$ is the normalized inductor impedance. Thus, from (7) and for a given maximum normalized peak-to-peak inductor current ripple, the minimum normalized inductor impedance is given by

$$X_{L_o,\,\min} = \frac{\pi}{f_{sw}} \frac{1}{\left(\dfrac{\Delta i_{L_o}}{i_{L_o}}\right)_{\max}}. \tag{8}$$

2) ***The capacitor $C_o$*** absorbs the triangular-shaped inductor current ripple defined by (6). The worst case, for design purposes, is when all the current ripple flows through the load capacitor. In this case, the peak-to-peak voltage ripple $\Delta v_{C_o}$ is defined by

$$\Delta v_{C_o} = \frac{1}{C_o}\, \frac{1}{2}\, \frac{\Delta i_{L_o}}{2}\, \frac{1}{4 f_{sw}}. \tag{9}$$

By using (2), (3), (6), and (9), the normalized peak-to-peak capacitor voltage can be expressed as

$$\frac{\Delta v_{C_o}}{v_{C_o}} = \frac{X_{C_o}}{X_{L_o}}\, \frac{\pi^2}{8 f_{sw}^2} \tag{10}$$

where $X_{C_o}$ is the normalized capacitor impedance and $X_{L_o}$ is the normalized inductor impedance chosen in (8). Thus, from (10) and for a given maximum normalized peak-to-peak capacitor voltage ripple, the maximum normalized capacitor impedance is obtained as

$$X_{C_o,\,\max} = X_{L_o}\, \frac{8 f_{sw}^2}{\pi^2} \left(\frac{\Delta v_{C_o}}{v_{C_o}}\right)_{\max}. \tag{11}$$

TABLE II
UPS COMPONENTS DESIGN AND SELECTION

| **Operating Conditions** | | |
|---|---|---|
| **Stage** | **Parameter** | **Value** |
| **Input** | voltage ($V_s$) | 85 V ÷ 110 V |
| | frequency ($f_{sw}$) | 60 Hz |
| **Load** | voltage ($V_l$) | 60 V, Trap. |
| | frequency ($f_l$) | 60 Hz |
| | power ($P_l$) | 500 W |
| **Battery Charger** | charging rate ($P_B$) | 50 W |
| | min. input voltage ($v_{ch,\min}$) | 80 V |
| **Inverter** | switching frequency ($f_{sw}$) | 40 kHz |

| **Design and Selection** | | | |
|---|---|---|---|
| **Component/Parameter** | **Criteria** | **Calculated** | **Actual** |
| **DC Link Capacitor ($C_{dc}$)** using (5) | $(\Delta v_{dc}/v_{dc})_{\max} = 0.20$ pu | 8.68 μF | 10 μF |
| **Load Filter Inductor ($L_o$)** using (8) | $(\Delta i_{Lo}/i_{Lo})_{\max} = 0.40$ pu | 225 μH | 250 μH |
| **Load Filter Capacitor ($C_o$)** using (11) | $(\Delta v_l/v_l)_{\max} = 0.01$ pu | 8.68 μF | 10 μF |
| **Bat. Charger Inp. Cap. ($C_{ch}$)** using (14) | $V_s = 85$ V | 103.52 μF | 100 μF |
| **Time Constant ($T_l$)** using (15) | $k = 2$ | 50 μs | 50 μs |

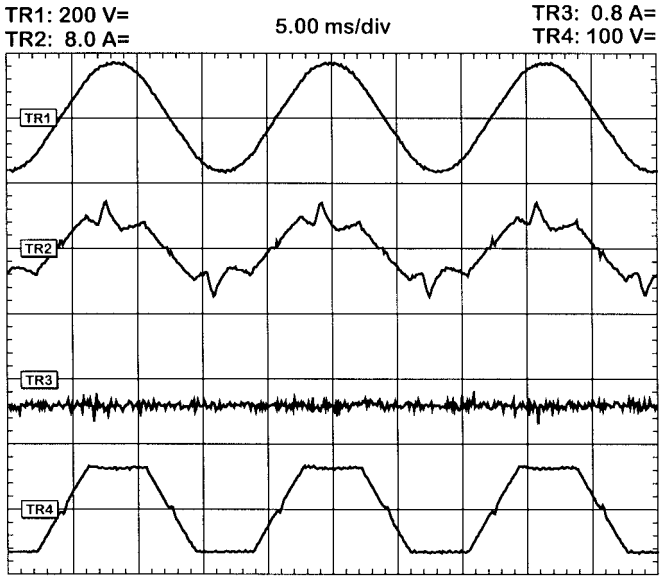


Fig. 8. *Normal/charging* operating mode (the ac mains supplies the load power—experimental waveforms). TR1: supply phase voltage ($v_s$). TR2: supply line current ($i_s$). TR3: battery current ($i_B$). TR4: load voltage ($v_l$).

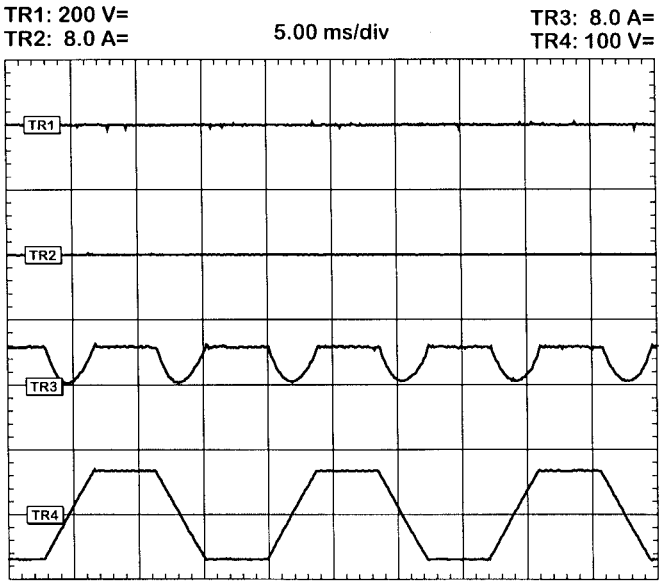


Fig. 9. *Backup* operating mode (the battery supplies the load power—experimental waveforms). TR1: supply phase voltage ($v_s$). TR2: supply line current ($i_s$). TR3: battery current ($i_B$). TR4: load voltage ($v_l$).

### C. The Battery-Charger DC-Input Capacitor ($C_{ch}$)

The battery-charger input voltage ($v_{C_{ch}}$), in the *normal/charging* operating mode, is as shown in Fig. 7(c). Note that the peak voltage is the peak dc-link voltage given by $\sqrt{2}V_s$, and the minimum voltage depends upon the capacitor size and charging rate of the battery. On the other hand, in the *backup* mode, the battery-charger input voltage is constant and defined by the actual battery voltage. Therefore, the battery-charger input capacitor value ($C_{ch}$) must ensure a minimum input voltage ($v_{C_{ch},\min}$) to allow the proper operation of the forward dc/dc converter in the *normal/charging* operating mode.

In this mode, energy is taken from the battery-charger input capacitor ($C_{ch}$) to charge the battery at constant current ($i_B$) and voltage ($v_B$). The energy absorbed ($\Delta E_a$) by the battery in one ac mains period is given by

$$\Delta E_a = v_B i_B t_{dis} \tag{12}$$

and the energy supplied ($\Delta E_s$) by the capacitor in one ac mains period is given by

$$\Delta E_s = \tfrac{1}{2} C_{ch}\left(\left(\sqrt{2}V_s\right)^2 - v_{ch,\min}^2\right). \tag{13}$$

To simplify the calculations, the losses are neglected, thus, both energies $\Delta E_s$ and $\Delta E_a$ are equal, and a maximum discharging time of one half of the ac mains period is assumed [$t_{dis} = 1/(2 \cdot f_{su})$]. Therefore, the maximum normalized capacitance for a given minimum battery-charger input voltage is given by

$$X_{C_{ch},\max} = \frac{2V_s^2 - v_{ch,\min}^2}{2\pi P_B} \tag{14}$$

where $X_{C_{ch},\max}$ is the normalized battery-charger input capacitor impedance and $P_B$ is the normalized charging power ($P_B = i_B v_B$).

### D. The Integrator Time Constant ($T_i$)

The time constant of the voltage regulator should be as small as possible in order to obtain a wide bandwidth. However, in order to maintain proper PWM operation, the slopes of the modulating waveform ($m$) should be smaller than those of the triangular carrier. Reference [8] establishes these mathematical constraints, which in practice result in the selection of an integral time constant between two to three times the switching period. Therefore

$$T_i = kT_{sw} \tag{15}$$

where $T_{sw}$ is the switching period and $k$ should be chosen between two and three.

## IV. Steady-State Performance

A laboratory prototype was implemented and designed upon the design guidelines presented in Section III. Table II shows the parameters and their calculated and actual values used in the setup in order to illustrate the static performance of the proposed UPS system: key waveforms (Figs. 8 and 9), input power factor [Fig. 10(a)], and the overall efficiency [Fig. 10(b)] were experimentally obtained for a resistive load.

To further prove the performance of the UPS, experimental waveforms for a nonlinear load are also included (Fig. 11). In this case, the load consists of a full-bridge rectifier supplying an $RC$ load.

### A. Key Experimental Waveforms

Fig. 8 shows the experimental waveforms for the *normal/charging* operating mode ($P_l = 400$ W, $V_s = 110$ V, and $R$ load). The load power is supplied by the ac mains (Fig. 8, TR2) as the battery is charged at constant power ($v_B = 100$ V,

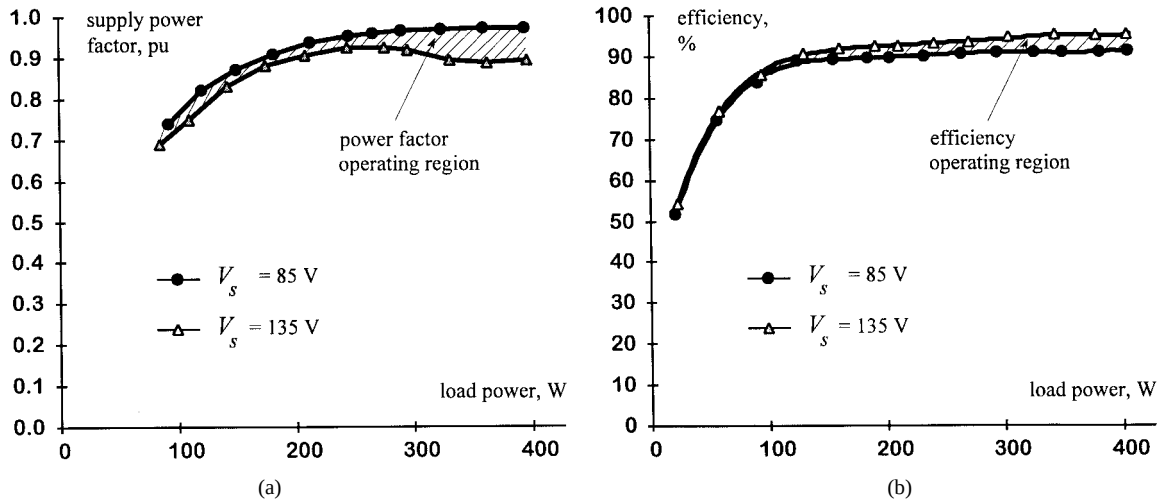


Fig. 10. UPS static performance as a function of the load power: (a) input power factor and (b) efficiency.

$i_B = 400$ mA). Note the negative polarity of the battery current (Fig. 8, TR3). The supply current is in phase with the phase voltage (Fig. 8, TR2) which ensures unity displacement power factor. The load voltage is trapezoidal ($v_l = 60$ V) as required (Fig. 8, TR4). It was also found that the supply line current spectrum presents low-amplitude harmonics all of which satisfy IEC 555.

Fig. 9 depicts the experimental waveforms for the *backup* operating mode ($P_l = 400$ W, $v_B = 96$ V, and $R$ load). The load power is supplied by the battery as indicated by the positive polarity of the battery current (Fig. 9, TR3). Like in the *normal/charging* operating mode, the load voltage is trapezoidal (Fig. 9, TR4).

### *B. Input Power Factor and Efficiency Evaluation*

Fig. 10(a) shows the experimental input power factor as a function of the load for the minimum and maximum supply voltages. At 400 W, the minimum power factor is 0.90 ($V_s = 135$ V), and the maximum power factor is 0.97 ($V_s = 85$ V). Finally, Fig. 10(b) shows the experimental efficiency as a function of the load for the minimum and maximum supply voltages. At 400 W, the minimum efficiency is 91% ($V_s = 85$ V) and the maximum is 94% ($V_s = 135$ V). These results confirm the high-static performance of the UPS system.

### *C. Key Experimental Waveforms for a Nonlinear Load*

The load in this case correspond to a full-bridge rectifier supplying an $RC$ load. Fig. 11 shows the experimental waveforms for the *normal/charging* operating mode ($P_l = 300$ W and $V_s = 110$ V). The supply current (Fig. 11, TR2) remains in phase with the supply voltage (Fig. 11, TR1) since the load current (Fig. 11, TR4) is in phase with the load voltage (Fig. 11, TR3). This feature ensures a unity displacement power factor. However, the distortion input power factor slightly increases as compared with the $R$ load case. For instance, in the case shown in Fig. 11, the overall input power factor decreases from 0.94 to 0.92. This is due to the fact that the load current does not have the trapezoidal shape of the $R$ load case, instead, it has a square shape, which is

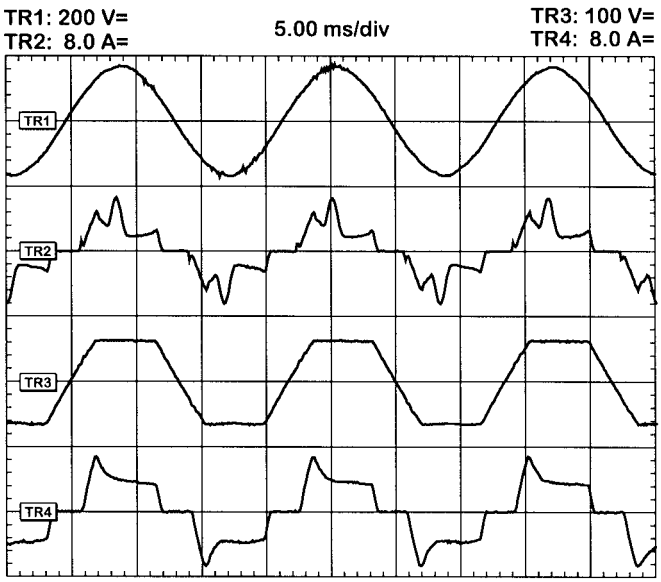


Fig. 11. *Normal/charging* operating mode for a nonlinear load. TR1: supply phase voltage ($v_s$). TR2: supply line current ($i_s$). TR3: load voltage ($v_l$). TR4: load current ($i_l$).

intrinsic to diode $RC$ loads. Nevertheless, it was also found that the supply-line-current spectrum presents low-amplitude harmonics all of which satisfy IEC 555.

Fig. 12 shows the experimental waveforms for the *backup* operating mode ($P_l = 300$ W and $v_B = 100$ V). The load voltage and current waveforms remain trapezoidal (Fig. 12, TR3) and square (Fig. 12, TR4), respectively. Thus, the applicability of the proposed UPS is confirmed for both *normal/charging* and *backup* operating modes for both $R$ and diode $RC$ loads. It was also found that the overall efficiency does not present appreciable differences between both load types and for both operating modes. Therefore, Fig. 10 is valid for both $R$ and diode $RC$ loads.

## V. Transient Performance

The transient performance of the proposed UPS is evaluated under three conditions for an $R$ load. These are: 1)

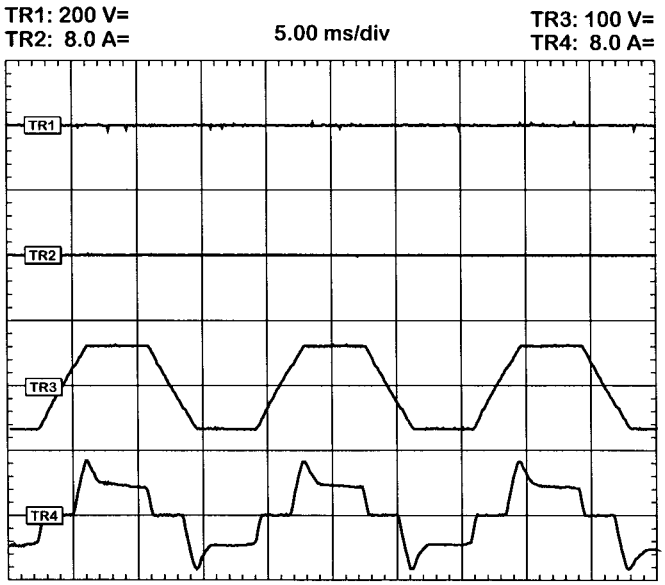


Fig. 12. *Backup* operating mode for a nonlinear load. TR1: supply phase voltage ($v_s$). TR2: supply line current ($i_s$). TR3: load voltage ($v_l$). TR4: load current ($i_l$).

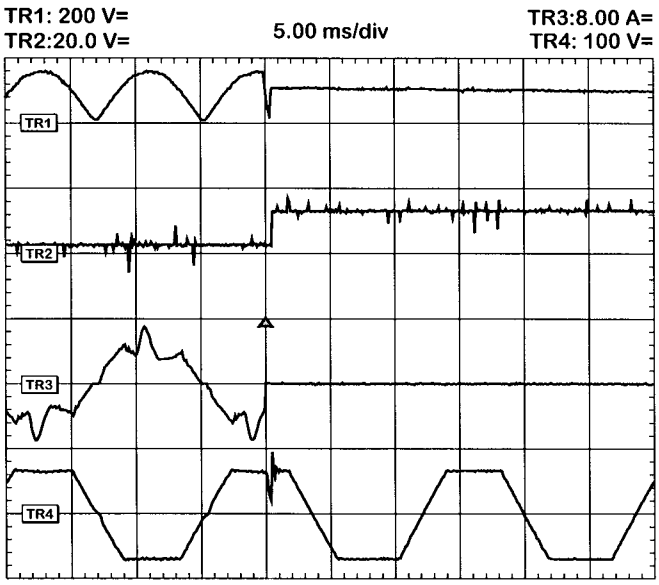


Fig. 13. AC supply to battery transition—experimental waveforms. TR1: dc voltage ($v_{\rm dc}$). TR2: battery switch on/off signal (SB). TR3: supply input current ($i_s$). TR4: load voltage ($v_l$).

supply–battery–supply transition; 2) load transient; and 3) supply-voltage transient.

### A. Supply–Battery–Supply Transition

Figs. 13 and 14 show key experimental waveforms associated with the *normal/charging* to *backup* and *backup* to *normal/charging* transitions, respectively. In the *normal/charging* to *backup* transition case, the ac supply distribution system fails, and thereby the *voltage supply detector block* enables the signal $S_B$ (Fig. 13, TR2). Thus, the battery takes over and power continuity to the load is ensured. The transition period takes around 500 $\mu$s, which ensures a reduced load-voltage distortion during the commutation (Fig. 13, TR4). Once the ac supply is back, the *supply-voltage detector block* waits until the *synchronization* and *reference generator block* get synchronized back with the ac supply and only then switch off the battery [$S_B$ (Fig. 14, TR2)]. During this period (60 ms), the load power is supplied by either the ac supply or the battery [whichever presents the highest dc voltage (Fig. 14, TR1)]. It can be observed that during the backup to *normal/charging* transition, the load voltage remains unaltered (Fig. 14, TR4).

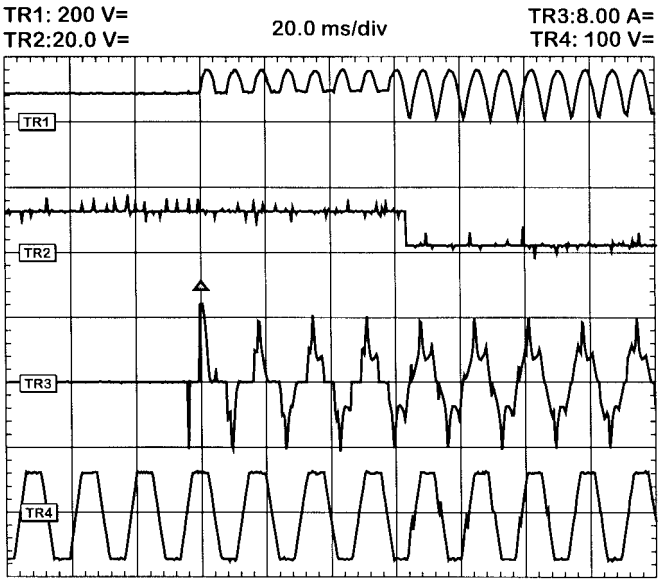


Fig. 14. Battery to ac supply transition—experimental waveforms. TR1: dc voltage ($v_{\rm dc}$). TR2: battery switch on/off signal ($S_B$). TR3: supply input current ($i_s$). TR4: load voltage ($v_l$).

### B. Load Transient

Fig. 15 shows the load current and voltage for a load step increase from 200 to 400 W. It can be observed that the load voltage (Fig. 15, TR2) presents an oscillation that features an undershoot of 25% and a settling time of about 500 $\mu$s.

A small-signal analysis of the UPS system (Appendix) indicates that the load-voltage transient, for a step up of the load power (or step down of the load resistance), can be modeled by

$$\Delta\tilde{v}_l = -\frac{L_o I_{L_o}}{R_l}\,\frac{\omega_r^2}{s^2 + 2\left(\dfrac{L_o}{2R_l}\,\omega_r\right)\omega_r s + \omega_r^2}. \qquad (16)$$

Equation (16) was used to simulate the load-voltage response for a 50% load step power @ 200 W. The zoom included in Fig. 15 shows both experimental and simulated responses. The results are in close agreement which validate the model. Therefore, from (16) and the experimental results, the additional observations can be made. First, the duration of the oscillation in (16) is only a function of the load filter resonant frequency ($t_r = 1/f_r = 2\pi/\omega_r = 314\,\mu$s, for $L_o = 250\,\mu$H, and $C_o = 10\,\mu$F). Also, although the damping factor [$\xi = L_o\omega_r/(2R_l)$] increases as the load power increases ($R_l \to 0$), the effective voltage undershoot increases since the gain in (16) increases. Finally, the load-voltage loop does not affect the transient oscillation [$k_f$ or $T_i$ are not in (16)], which

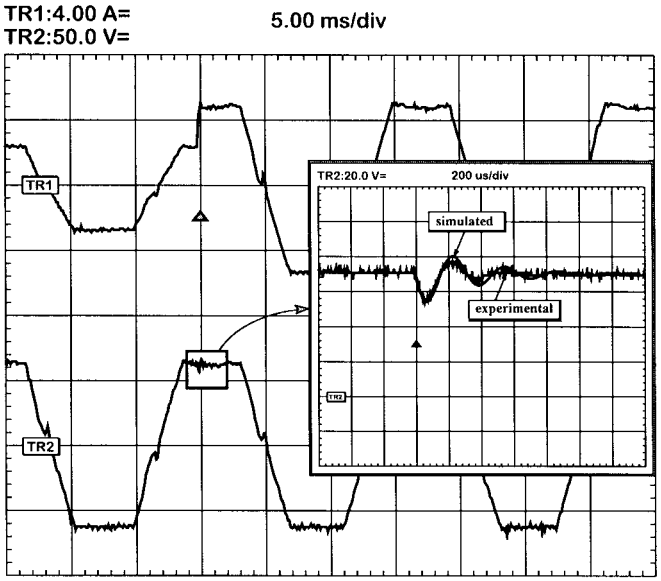


Fig. 15. Load step transient (from 200 to 400 W—experimental waveforms). TR1: load current ($i_l$). TR2: load voltage ($v_l$).

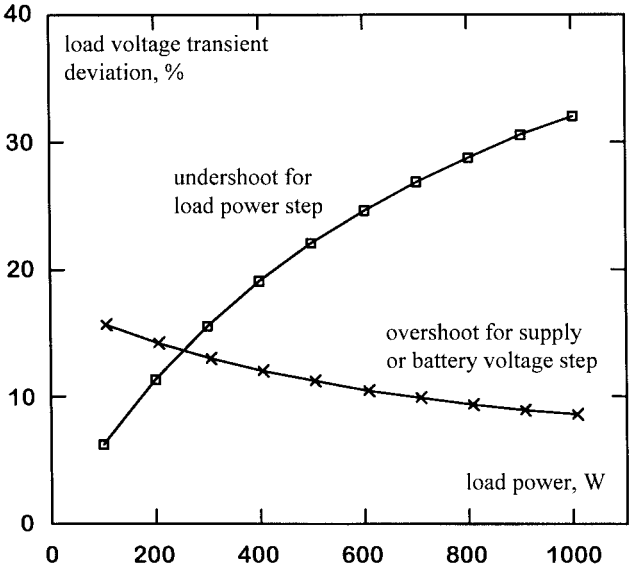


Fig. 16. Normalized load-voltage transient deviation for 50% step variation of the load power (**) and supply/battery voltage (**).

is due to the fact that the feedback signal is actually taken from the ac side of the inverter (Fig. 2) and not from the load itself.

Fig. 16 depicts the theoretical load-voltage undershoot that is obtained using (16) for 50% load step up at different load power levels. The overshoot of the load voltage included in Fig. 15 confirms the theoretical analysis.

### *C. AC Supply/Battery-Voltage Transient*

A 50% supply-voltage step increase was performed to test the UPS system performance under supply-voltage variations. Fig. 17 shows the experimental supply and load voltage for the above condition. The load voltage (Fig. 17, TR2) presents a very slight oscillation. This proves the UPS capability to reject the supply-voltage variations.

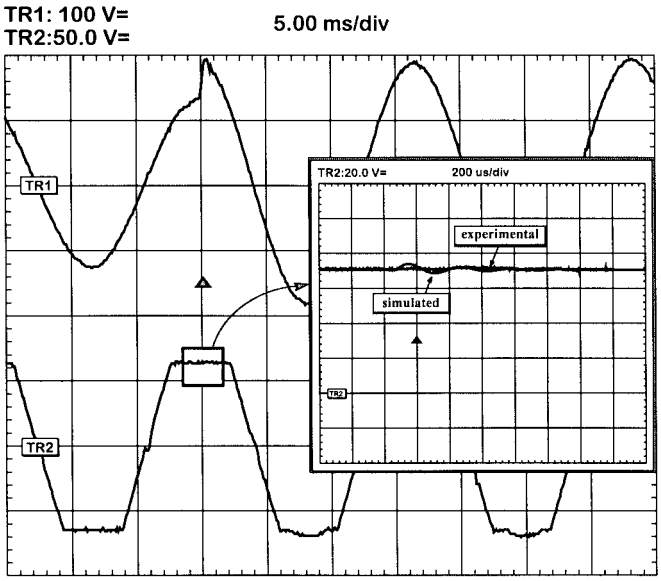


Fig. 17. AC supply-voltage transient (85–135-V step increase at 400-W output—experimental waveforms). TR1: supply voltage ($v_s$). TR2: load voltage ($v_l$).

The small-signal analysis of the UPS system (Appendix) indicates that the load voltage for a step up of the supply or battery voltage can be modeled by

$$\Delta\tilde{v}_l = \frac{M}{A_\Delta}\,\frac{\omega_r^2}{\left(s+\dfrac{k_f\,V_{\rm dc}}{T_i\,A_\Delta}\right)\left\{s^2+2\left(\dfrac{L_o}{2R_l}\,\omega_r\right)\omega_r s+\omega_r^2\right\}}. \tag{17}$$

Equation (17) contains the same second-order transient response as (16). Therefore, load transient oscillations of the order of at most 500 $\mu$s are predicted. The model of the transient response (17) also exhibits an additional pole as a result of the load-voltage feedback loop. This extra root provides additional damping that guarantees lower load-voltage transient deviations under supply- or battery-voltage variations as compared to load power transients. Fig. 16 depicts the theoretical load-voltage overshoot that is obtained using (17) for 50% supply/battery-voltage step up at different load power levels. The zoom of the load-voltage oscillation included in Fig. 17 shows that the experimental oscillatory response (4% of overshoot, see zoom in Fig. 17) is more damped than the predicted one (12% of overshoot, see Fig. 16 @ 400 W). This discrepancy can be explained as a result of the finite slope of the step increase in the supply voltage achieved in the experimental tests (Fig. 17).

## VI. Conclusion

A single-stage UPS system for a single-phase trapezoidal-shaped ac-voltage supply has been presented and evaluated under different steady-state and transient conditions. Steady-state tests using resistive (linear) and diode $RC$ (nonlinear) loads have shown that the UPS system presents high-input power factor (0.94, at nominal voltage) and high efficiency (93%, at nominal voltage). Moreover, in both cases the supply current spectrum presents low-order harmonics, all of which

satisfy IEC 555. The additional transient tests are: 1) supply to battery transition; 2) battery to supply transition; 3) load transient; and 4) supply-voltage transient. These tests show that: 1) the transition from the ac supply to battery is done in 500 $\mu$s; 2) for the most severe transient conditions (step load variation), the load voltage features an oscillation of at most 500 $\mu$s; and 3) under supply/battery-voltage step variations, an additional source of damping is provided by the instantaneous load-voltage loop that ensures load-voltage overshoots of at most 15%. A 1-kVA laboratory unit was implemented and designed to perform the various tests.

## APPENDIX
## SMALL-SIGNAL ANALYSIS OF THE LOAD VOLTAGE VERSUS THE LOAD POWER AND SUPPLY-VOLTAGE VARIATIONS FOR RESISTIVE LOADS

From Figs. 2 and 5(a), the PWM inverter, output filter, and $R$ load can be modeled by

$$m = \frac{1}{T_i}\int_{-\infty}^{t}(v_{o,\mathrm{ref}} - k_f v_o)\,d\tau \tag{18}$$

$$v_o = L_o\frac{di_{L_o}}{dt} + v_l \tag{19}$$

$$i_{L_o} = C_o\frac{dv_l}{dt} + \frac{v_l}{r_l} \tag{20}$$

where

| | |
|---|---|
| $m$ | modulating waveform; |
| $v_{o,\mathrm{ref}}$ | output-voltage reference; |
| $v_o$ | actual output voltage; |
| $i_{L_o}$ | inductor current; |
| $v_l$ | load voltage; |
| $L_o$ | load filter inductor; |
| $C_o$ | load filter capacitor; |
| $T_i$ | integrator time constant; |
| $r_l$ | load resistance. |

Since a carrier-based PWM technique is used, the output voltage can be approximated by $v_o = mv_{\mathrm{dc}}/A_\Delta$, and, thereby, the model of the system (18)–(20) can be rewritten as

$$\frac{dm}{dt} = \frac{1}{T_i}v_{o,\mathrm{ref}} - \frac{k_f}{T_i A_\Delta}mv_{\mathrm{dc}} \tag{21}$$

$$\frac{di_{L_o}}{dt} = \frac{1}{L_o A_\Delta}mv_{\mathrm{dc}} - \frac{1}{L_o}v_l \tag{22}$$

$$\frac{dv_l}{dt} = \frac{1}{C_o}i_{L_o} - \frac{1}{r_l C_o}v_l \tag{23}$$

where $A_\Delta$ is the triangular-carrier amplitude and since $C_{\mathrm{dc}}$ is very small, $v_{\mathrm{dc}}$ is the actual rectified supply voltage or battery voltage, depending on the UPS operating mode. The resulting model (21)–(23) is nonlinear, and, therefore, a small-signal approach is used. If the system state variable vector is $\mathbf{x} = [mi_{L_o}v_l]^T$, the system perturbation vector is defined as $\mathbf{u} = [r_l v_{\mathrm{dc}}]^T$, and the output $\mathbf{y} = [v_l]$, the small-signal model is

$$\frac{d\Delta\tilde{\mathbf{x}}}{dt} = \mathbf{A}\,\Delta\tilde{\mathbf{x}} + \mathbf{B}\,\Delta\tilde{\mathbf{u}} \quad \Delta\tilde{\mathbf{y}} = \mathbf{C}\Delta\tilde{\mathbf{x}} \tag{24}$$

where

$$\mathbf{A} = \begin{bmatrix} \dfrac{-k_f V_{\mathrm{dc}}}{T_i A_\Delta} & 0 & 0 \\ \dfrac{V_{\mathrm{dc}}}{L_o A_\Delta} & 0 & \dfrac{-1}{L_o} \\ 0 & \dfrac{1}{C_o} & \dfrac{-1}{R_l C_o} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} 0 & \dfrac{-k_f M}{T_i A_\Delta} \\ 0 & \dfrac{M}{L_o A_\Delta} \\ \dfrac{I_{L_o}}{R_l C_o} & 0 \end{bmatrix}$$

where $\mathbf{C} = [0\ 0\ 1]$, $\Delta\tilde{\mathbf{x}}$, $\Delta\tilde{\mathbf{u}}$, and $\Delta\tilde{\mathbf{y}}$ are the small variations of the state variable, perturbation, and output vectors, respectively, $V_{\mathrm{dc}}$ is the dc-link voltage, $R_l$ is the load resistor, $M$ is the modulation index, and $I_{L_o}$ is the load inductor current in the operation point. Note that in order to consider load power variations, the resistive load has been assumed $r_l = R_l + \Delta\tilde{r}_l$.

The Laplace transform is used to solve (24). Thus

$$\Delta\tilde{\mathbf{y}} = \begin{bmatrix} \dfrac{L_o I_{L_o} s}{s^2 R_l L_o C_o + sL_o + R_l} \\ \dfrac{R_l T_i M s}{(sT_i A_\Delta + k_f V_{\mathrm{dc}})(s^2 R_l L_o C_o + sL_o + R_l)} \end{bmatrix}^T \Delta\tilde{\mathbf{u}}. \tag{25}$$

Therefore, the load voltage as a function of the load power (or load resistance) variation is given by

$$\Delta\tilde{v}_l = \frac{L_o I_{L_o}}{R_l}\,\frac{\omega_r^2 s}{s^2 + 2\left(\dfrac{L_o}{2R_l}\omega_r\right)\omega_r s + \omega_r^2}\,\Delta\tilde{r}_l \tag{26}$$

and the load voltage as a function of the supply- or battery-voltage variation is given by

$$\Delta\tilde{v}_l = \frac{M}{A_\Delta}\,\frac{\omega_r^2 s}{\left(s + \dfrac{k_f V_{\mathrm{dc}}}{T_i A_\Delta}\right)\left\{s^2 + 2\left(\dfrac{L_o}{2R_l}\omega_r\right)\omega_r s + \omega_r^2\right\}} \cdot \Delta\tilde{v}_{\mathrm{dc}} \tag{27}$$

where $\omega_r$ is the load filter angular resonance frequency defined as $\omega_r^2 = 1/L_o C_o$.

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