A Current-Source-Inverter-Fed Induction Motor Drive System with Reduced Losses

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***Abstract*—Standard low- and medium-power induction motor drives are based on the pulsewidth modulation (PWM) voltage-source inverter fed from a diode rectifier. The dual topology, based on the current-source inverter/rectifier structure is used in medium- and high-power applications. This paper analyzes the existing motor drives based on current-source topologies and proposes a control strategy that addresses some of the drawbacks of this approach compared to the voltage-source approach. The proposed strategy features the following: 1) an on-line operated PWM inverter, using instantaneous output capacitor voltage control based on space-vector modulation and 2) an additional inverter modulation index control loop, ensuring constant inverter modulation index and minimum dc-link current operation. The resulting additional advantages include the following: 1) fixed and reduced motor voltage distortion; 2) minimized dc-bus inductor losses; 3) minimized switch conduction losses; and 4) elimination of motor circuit resonances. Experimental results based on a digital signal processor implementation are given.**

***Index Terms*—AC drive, pulsewidth modulation current-source rectifier/inverter, reduced losses.**

I. Introduction

TO CONTROL the motor armature, ac adjustable-speed induction motor drives employ mostly a voltage-source inverter (VSI) topology. Both scalar and vector control of induction motors are used in this approach, the latter requiring current control of the VSI [1]. Although energy storage is more practical and efficient in capacitors than in inductors, the use of VSI's may result in reduced drive reliability due to the high dv/dt of the pulsewidth modulated inverter output voltage [2]. However, the dv/dt can be significantly lowered by filtering the VSI output voltage. This can be achieved by adding filtering reactors, or better, *LC* filters.

The current-source inverter (CSI) topology offers a number of inherent advantages, including [3]: 1) short-circuit protection, the output current being limited by the regulated dc-bus current; 2) low output voltage dv/dt, resulting from the filtering effect of the output capacitor; 3) high converter reliability, due to the unidirectional nature of the switches and the inherent short-circuit protection; and 4) instantaneous and continuous regenerative capabilities. These features, in addition to the availability of large reverse blocking devices [such as gate-turn-off thyristors (GTO's)], make the CSI-based drive attractive in medium to high power applications.

Despite the above advantages, the configuration based on a thyristor front-end rectifier presents a poor and variable overall input power factor (PF). To overcome this drawback, it has been proposed to replace the front-end thyristor rectifier by a pulsewidth modulation (PWM) current-source rectifier. This allows operation with a unity input displacement PF, while preserving the regenerative capabilities of the drives [4].

However, the implementation of CSI drive systems with on-line control capabilities is more complex than for VSI's, due to the CSI gating requirements. This has resulted in the widespread use of selective harmonic elimination (SHE) stored patterns [3], [5], [6], usually with a fixed modulation index. On-line control of the CSI requires complex control [3] and/or power [7] circuitry, which has led to two main control approaches: 1) control schemes that use stored patterns (such as SHE) and variable dc-link current to control the output current and 2) control schemes that use fixed dc-link current and a variable modulation index of the PWM generator at the CSI stage to control the output current. However, the first approach presents possible potential resonances between the output filter capacitor and the motor inductances [8], [9], and the second approach features the following [10], [11]: 1) important losses in the power switches and dc-link inductor; 2) power switches under constant current stress (they must always commutate the nominal dc-link current); and 3) variable harmonic distortion of the motor voltage with the CSI modulation index.

This paper discusses a CSI-based ac induction machine drive with the following features: 1) the motor voltage, rather than the motor current, is regulated on-line by using a feedback control technique and 2) the dc-link current is regulated to the minimum value required to keep the inverter modulation index constant and independent of the speed reference and load torque. Furthermore, other features include the following: 1) the entire control strategy is implemented in a digital signal processor (DSP) system, based on the TMS320C30 chip; 2) the overall speed control strategy is based on a constant voltage/frequency (V/f) scalar control technique; 3) both rectifier and inverter stages are PWM and space-vector modulated. The above features lead to the following advan-

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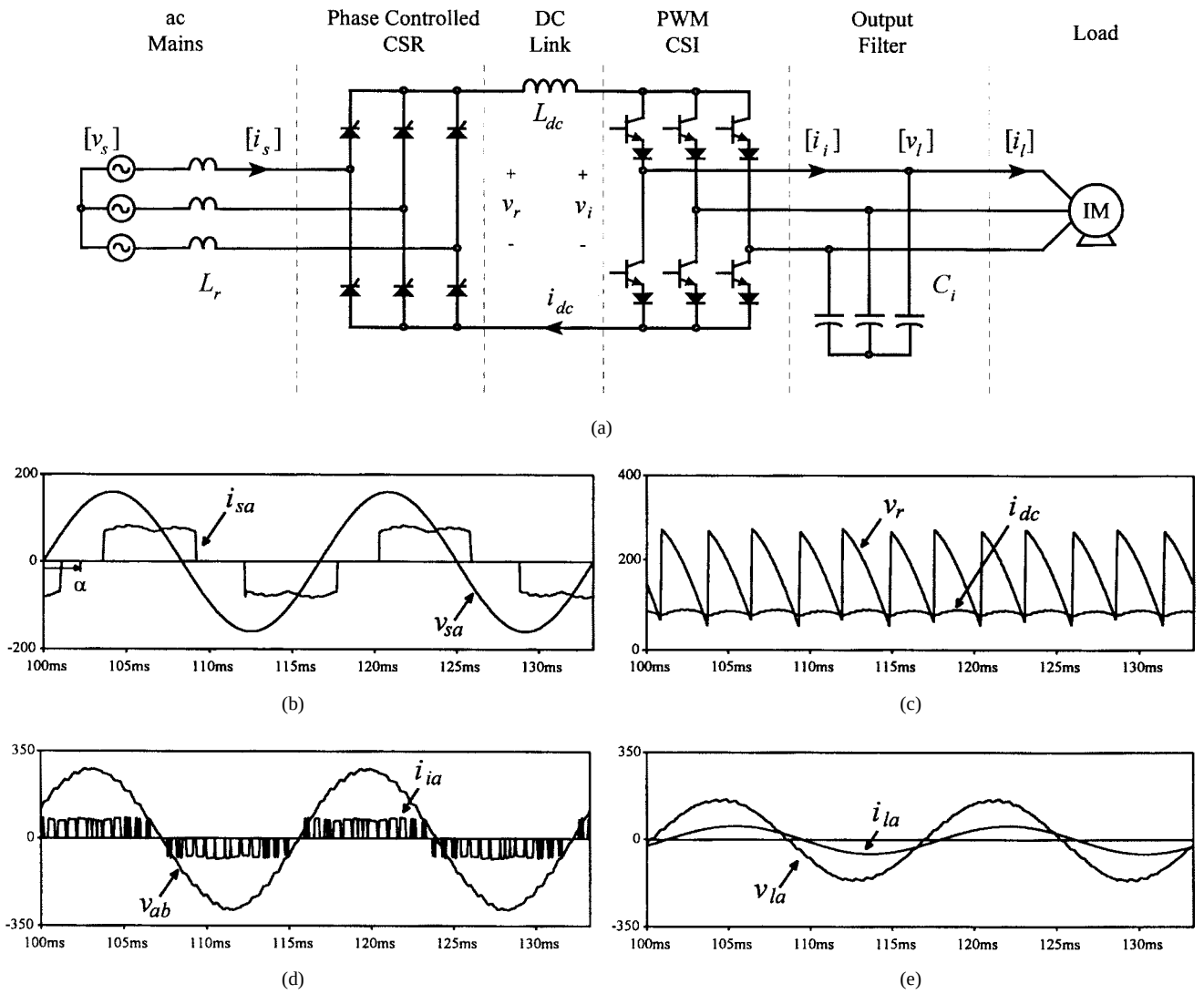

Fig. 1. AC drive CSI based on a phase-controlled front-end rectifier (50% nominal load and 60-Hz output). (a) Power topology. (b) Supply phase voltage (v_{sa}) and supply line current $(15 \cdot i_{sa})$. (c) DC rectifier voltage (v_r) and dc-link current $(15 \cdot i_{\rm dc})$. (d) CSI line current (i_{ia}) and load line voltage (v_{ab}). (e) Load phase voltage (v_{la}) and load line current $(15 \cdot i_{la})$.

tages over conventional CSI motor drive implementations: 1) the gating signals are directly generated by the space-vector digital modulator (extra circuitry is only necessary to ensure overlaps); 2) the potential resonances are eliminated due to the feedback-based voltage controller; 3) the stresses on power switches and the overall losses are always minimum due to the minimum dc-link current operation; and 4) due to the constant inverter modulation index operation, the motor voltage harmonic distortion is constant, which minimizes the induction motor losses and allows an accurate output filter design. These features make the CSI drive an interesting alternative to VSI-based drives operating at similar switching frequency, when the requested fundamental reactive power could be disregarded with respect to output power.

A complete comparison with standard CSI-based ac drives is also presented. Key performance indices, such as harmonic distortion (THD), PF, and time response are evaluated and tabulated for both the standard and the proposed schemes. Experimental results are given for a 2-kVA induction motor drive.

II. Standard CSI-Based AC Drives

In this paper, drive classification is based on the structure of the front-end power converter, which could be either a phase-controlled thyristor rectifier or a PWM current-source rectifier.

A. Phase-Controlled Front-End Rectifiers

These drives use a front-end rectifier based on thyristor-type power switches (Fig. 1), which can be operated with either variable or fixed dc-link current. The performance of the drive converter depends on this last feature.

1) Variable DC-Link Current Scheme The CSI is operated with a fixed pattern, which is usually optimized in terms of harmonic spectrum and switching frequency. Thus, the load voltage harmonic distortion (THD_v) is minimum and constant (Table I). However, the dc-link current must be adjusted through transient changes in firing angle (α) to meet the requirements of the load. The dc voltage, on the other hand, is practically constant and independent of the load torque.

TABLE I
CSI-BASED AC DRIVE SCHEME COMPARISON

Parameter	Thyristor Front-end Rectifier		PWM Front-end Rectifier	
	Variable i_{dc} Fixed CSI Pattern	Fixed i_{dc} PWM CSI	Fixed i_{dc} PWM CSI	Variable i_{dc} PWM CSI *
THD_v, motor voltage harmonic distortion	speed dependent $10 < THD_v < 3.5\ \%$	speed dependent $10 < THD_v < 3.5\ \%$	speed dependent $10 < THD_v < 3.5\ \%$	constant $THD_v = 3.5\%$
THD_i, supply current harmonic distortion	constant $THD_i = 142\%$	constant $THD_i = 142\%$	speed-torque dep. $10 < THD_i < 3.5\ \%$	constant $THD_i = 3.5\%$
ac supply power factor (pf)	speed dependent $0 < pf < 0.85$	speed-torque dep. $0 < pf < 0.85$	speed-torque dep. $0.8 < pf < 0.95$	constant $pf = 0.95$
transient response τ	slow $\tau \alpha\ 1/L$	fast $\tau \alpha\ 1/f_{sample}$	fast $\tau \alpha\ 1/f_{sample}$	fast $\tau \alpha\ 1/f_{sample}$
dc bus and switch conduction losses	reduced	high	high	minimized

*: Proposed CSI-based ac drive control scheme.

$$\text{where, } THD_v\% = \frac{\sqrt{\sum_{k=2}^{\infty} V_{lk}^2}}{V_{l1}} \cdot 100 \quad \text{and} \quad THD_i\% = \frac{\sqrt{\sum_{k=2}^{\infty} I_{sk}^2}}{I_{s1}} \cdot 100$$

This last feature leads to a constant input current displacement factor and, thereby, a constant overall PF (Table I). Also, since the dc-link current tracks the output current, the dc-bus and switch conduction losses are kept to a minimum. Usually, the dc-link inductor is designed to have an acceptable current ripple (5%). In order to achieve this value and due to the low-order harmonics produced by the thyristor rectifier (sixth, 12th, etc.), the size of the dc inductor becomes quite bulky. This results in a slow system transient response. Also, the supply current has a high distortion factor $(\text{THD}_i = 142\%)$ due to the low-order harmonics (fifth, seventh, etc.) injected by the thyristor rectifier. Fig. 1 shows typical waveforms of the converter. The rectifier phase angle (α) is only adjusted during transient conditions occurring under load speed and torque variations.

2) Fixed DC-Link Current Scheme Unlike the above control scheme, the CSI is operated with a PWM pattern, which varies as a function of the CSI modulation index. Therefore, the load voltage harmonic distortion (THD_v) is variable and depends upon the speed and load torque (Table I). Since the dc-link current is fixed, the different load power requirements are obtained by varying the dc-link voltage. To achieve this, the input current displacement factor is continuously adjusted and, thereby, the input PF becomes variable and close to zero for light loads. Contrary to the variable dc-link current scheme, the dc-bus and switch conduction losses are always maximum, due to the fact that the dc-link current is always maximum (Table I). Although the dc-link inductor size is as big as the one used in the above scheme, the dynamic response of the load current is improved, due to the variable PWM pattern approach with time responses to modulation index changes of the order of a sampling period. This scheme also presents a high supply current harmonic distortion, due to the thyristor rectifier operation (Table I). Typical waveforms shown in Fig. 1 are also applicable in this case; however, in this mode of operation, the rectifier phase angle (α) is continuously adjusted to maintain a constant dc-link current, regardless of the load speed and torque.

B. PWM Front-End Rectifiers

Unlike phase-controlled rectifier topologies, this topology uses a PWM rectifier (Fig. 2). This allows a reduction in the harmonics injected into the ac supply. The rectifier is operated with a fixed dc-link current. Fig. 2 shows typical waveforms of the converter. The PWM pattern is adjusted on a continuous basis to keep a constant dc-link current. In contrast to topologies based on thyristor front-end rectifiers, the overall drive input PF is always greater than 0.95, and the total input current harmonic distortion, which depends on the sampling frequency, is typically lower than 10% (Table I). Also, since the output inverter is PWM modulated, the system has time responses close to the sampling period. However, the dc-bus losses and switch conduction losses are maximum, since the dc-link current is always equal to its maximum value, regardless of the load speed and torque.

III. PROPOSED AC DRIVE SYSTEM DESCRIPTION

A. Power Circuit

The complete power circuit (Fig. 2) belongs to the second category described above, therefore, it is composed of a three-phase PWM rectifier, a dc-link reactor, and a three-phase PWM CSI.

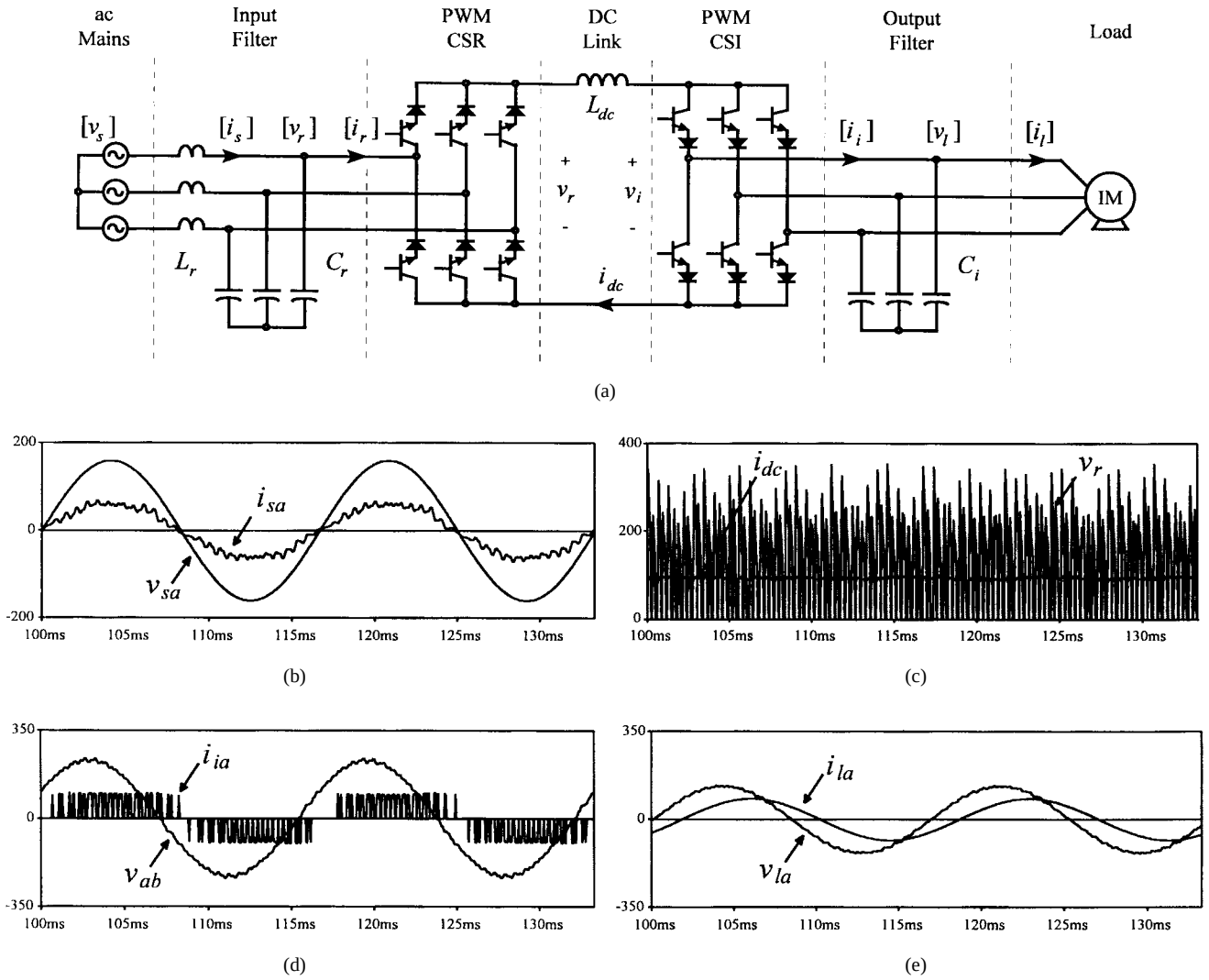

Fig. 2. AC drive CSI based on a PWM front-end rectifier (50% nominal load and 60-Hz output). (a) Power topology. (b) Supply phase voltage (v_{sa}) and supply line current $(15 \cdot i_{sa})$. (c) DC rectifier voltage (v_r) and dc-link current $(15 \cdot i_{\rm dc})$. (d) CSI line current (i_{ia}) and load line voltage (v_{ab}). (e) Load phase voltage (v_{la}) and load line current $(15 \cdot i_{la})$.

The main function of the PWM rectifier is to regulate the level of the dc-link current $(i_{\rm dc})$, by transiently adjusting the PWM rectifier dc voltage (v_r). The high-frequency harmonics injected into the ac mains by the PWM rectifier operation are easily absorbed by the rectifier filter (C_r). Therefore, the input distortion PF and, thereby, the overall input PF, is close to unity over the whole operating range.

The second system component is the dc-link reactor $(L_{\rm dc})$. Its function is to smooth the dc-link current $(i_{\rm dc})$ and, therefore, act as a current source to the PWM CSI. The magnitude of $L_{\rm dc}$ depends on the permissible dc-link current ripple and the switching frequencies of the PWM rectifier and PWM CSI. Since practical switching frequencies are of the order of 1–10 kHz, the size of the dc-link inductor becomes substantially smaller than for the thyristor rectifier case.

Finally, the CSI produces three-phase PWM line currents $([i_l])$ with the minimum possible harmonic distortion. The output capacitive filter (C_i) absorbs the high-frequency current harmonics generated by the CSI PWM action and, thereby, defines the sinusoidal output voltage.

B. Control System Structure

The general control diagram of the proposed CSI-based ac drive is shown in Fig. 3. Unlike the fixed dc-link current scheme, this scheme varies the dc-link current, in order to keep the CSI modulation index constant in steady state. The global control strategy is composed of two main control loops.

The first control loop is the motor speed control (ω_m) based on a slip speed regulator, which sets the slip speed reference $(\omega_{\rm sl})$. The synchronous speed $(\omega_{\rm ms})$, obtained by adding the actual speed and the slip speed, determines the inverter frequency (f_l). The motor voltage reference signal $(V_{l,\rm ref})$ is constructed from the frequency using a function generator, which ensures a nearly constant flux operation. Finally, the voltage controller and the space-vector modulator produce the switching pattern $([S_i])$ based on the difference between the sine voltage reference waveforms $([v_{l,\rm ref}])$ and the sampled load voltage waveforms $([v_l])$. This feedback scheme ensures that the CSI gating pattern is modified on-line, so as to force the output voltage $[v_l]$ to track the reference $[v_{l,\rm ref}]$, thereby resulting in a fast dynamic response, with rise times in

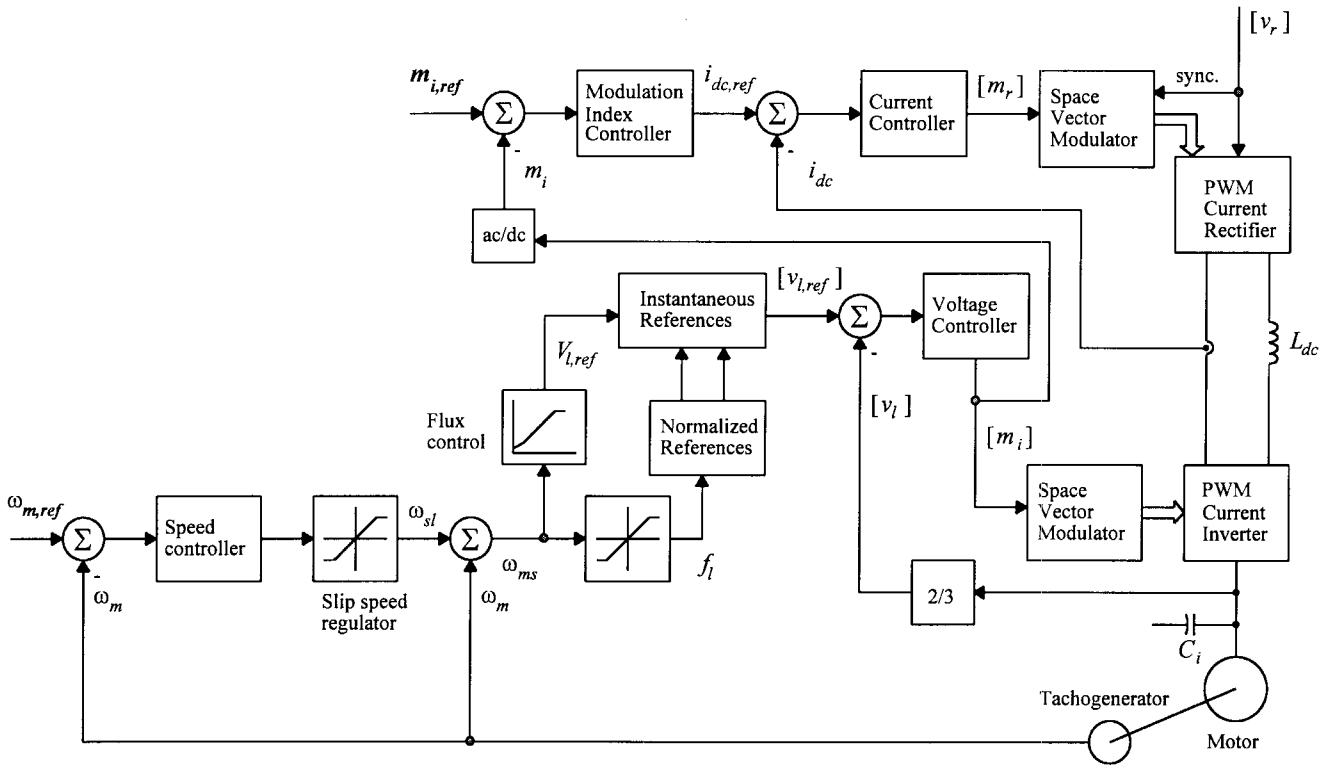

Fig. 3. Control scheme of the proposed ac drive CSI incorporating modulation index control for reduced losses (motor control uses the V/f scheme).

the range of the sampling period (t_{sample}) of the space-vector technique. Analysis and design guidelines of this inner motor voltage loop are given in [12].

The second control loop is the PWM CSI modulation index loop (m_i). The main function of this slower loop is to set on-line the dc-link current reference $(i_{\text{dc,ref}})$ in such a way that the steady-state PWM CSI modulation index remains equal to the reference $(m_{i,\text{ref}})$. The next section demonstrates theoretically that, by properly adjusting the dc-link current, the modulation index of the CSI can be effectively regulated.

IV. The Modulation Index Control Loop

This loop is designed to be slower than the dc-link current and the motor voltage loops. This feature allows one to consider that the actual dc current and actual motor voltages are equal to their respective references when analyzing the dynamic of the modulation index loop. Thus, the dc-link stage can be modeled by a pure current source with a value equal to the reference $(i_{\text{dc,ref}})$ and the CSI dc-bus voltage approximated by

$$v_i = m_{ia} v_{la,\text{ref}} + m_{ib} v_{lb,\text{ref}} + m_{ic} v_{lc,\text{ref}} \tag{1}$$

where m_{ia}, m_{ib}, and m_{ic} are the time-average modulating signals generated by the space-vector modulation technique, and $v_{la,\text{ref}}$, $v_{lb,\text{ref}}$, and $v_{lc,\text{ref}}$ are the motor phase voltage references. Since the motor voltages references and the modulating signals are sinusoidal quantities, they can be represented by

$$\begin{bmatrix} m_{ia} \\ m_{ib} \\ m_{ic} \end{bmatrix} = m_i \begin{bmatrix} \sin(\omega_l t) \\ \sin(\omega_l t - 120^\circ) \\ \sin(\omega_l t - 240^\circ) \end{bmatrix} \tag{2}$$

and

$$\begin{bmatrix} v_{la} \\ v_{lb} \\ v_{lc} \end{bmatrix} = \sqrt{2}\frac{V_l}{\sqrt{3}} \begin{bmatrix} \sin(\omega_l t - \psi) \\ \sin(\omega_l t - 120^\circ - \psi) \\ \sin(\omega_l t - 240^\circ - \psi) \end{bmatrix} \tag{3}$$

where m_i is the CSI modulation index, V_l is the motor line rms voltage, ω_l is the motor voltage frequency, and ψ is an angle which depends upon the operating conditions and system parameters. Using (2) and (3), the CSI dc-bus voltage (1) can be rewritten as

$$v_i = \sqrt{\frac{3}{2}} m_i V_l \cos(\psi). \tag{4}$$

If the CSI and the output filter are considered lossless, the CSI instantaneous power balance indicates that

$$v_i i_{\text{dc,ref}} = \sqrt{\frac{3}{2}} m_i i_{\text{dc,ref}} V_l \cos(\psi) = p_l \tag{5}$$

where p_l is the load power. Equation (5) shows that, in order to control the load power, either the dc-link current $(i_{\text{dc,ref}})$ or the CSI modulation index (m_i) can be adjusted. In this paper, a combination of the two quantities is used in a cascade strategy (Fig. 2). Transient changes in the load are accommodated by adjusting the CSI modulation index through the inner motor voltage loop. In addition, the slower CSI modulation index outer loop adjusts the dc-link current to maintain the CSI modulation index to a high value under steady-state conditions. It can also be seen from (5) that, by maximizing the modulation index, the dc-link current is minimized. These features and their effect are evaluated experimentally in the next section.

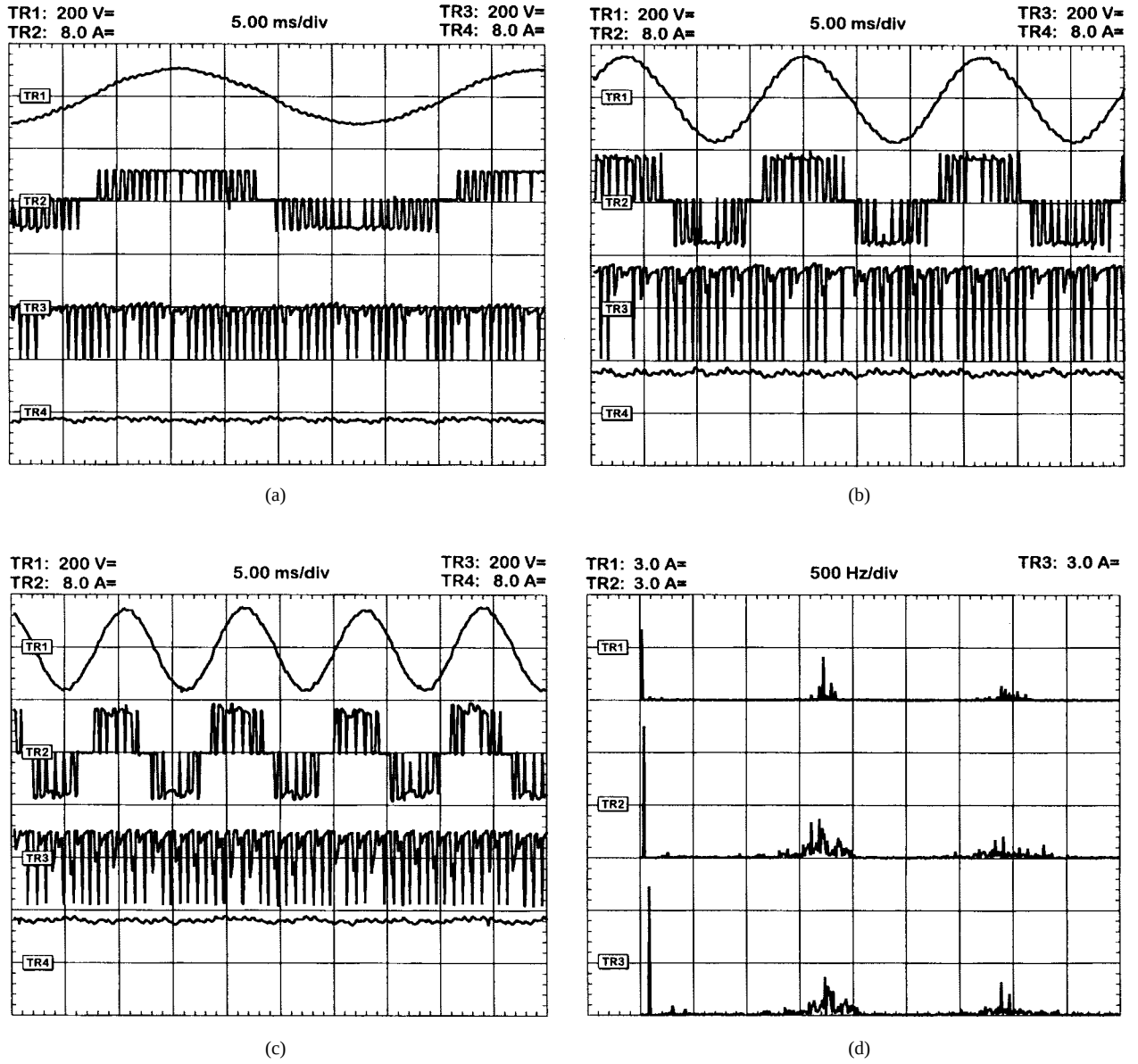

Fig. 4. Experimental waveforms for the proposed CSI-based ac drive. (a) 30-Hz operation. (b) 60-Hz operation. (c) 90-Hz operation. (*TR1*: motor line voltage (v_{ab}); *TR2*: CSI line current (i_{ia}); *TR3*: CSI dc-bus voltage (v_i); *TR4*: dc-link current (i_{dc}).) (d) CSI line current spectrum (i_{la}). (*TR1*: 30-Hz operation; *TR2*: 60-Hz operation; *TR3*: 90-Hz operation.)

It should be noted that a high modulation index set point under steady-state conditions (M_i near 1.0) is desired, in order to minimize the dc-link current and to obtain low harmonic distortion waveforms on the load side. However, a lower modulation index would provide a wider operating range before the CSI modulator goes into saturation $(M_i > 1.0)$ under transient conditions. When the modulation index reaches its maximum, the slower acting modulation index controller will increase the dc-link current to meet the load requirements. The converter then operates as a standard fixed dc-bus current CSI drive. This is an intrinsic limitation of the proposed control strategy. Simulation and experimental studies have shown that a modulation index equal to 0.8 provides a good compromise between steady-state and transient operation requirements. Specifically, this set point provides a 20% transient current increase before the CSI modulator goes into saturation.

The linearization of (5) gives

$$\Delta m_i = -\frac{M_i}{I_{\mathrm{dc,ref}}}\Delta i_{\mathrm{dc,ref}} + \frac{M_i}{P_l}\Delta p_l \tag{6}$$

where M_i, P_l, and $I_{\mathrm{dc,ref}}$ are the values of m_i, p_l, and $i_{\mathrm{dc,ref}}$ at the operating point, and Δm_i, Δp_l, and $\Delta i_{\mathrm{dc,ref}}$ are the small deviations of m_i, p_l, and $i_{\mathrm{dc,ref}}$ around the operating point. Note that Δp_l becomes a perturbation and M_i, P_l, and $I_{\mathrm{dc,ref}}$ are obtained from (5) evaluated at the operating point. The small-signal model (6) shows an inverse relation between the dc-link current and the CSI modulation index. Therefore, a linear controller with a negative gain can provide the necessary compensation to obtain a stable closed loop. In this paper, a proportional integral (PI) controller ten times slower than the output voltage loop is implemented.

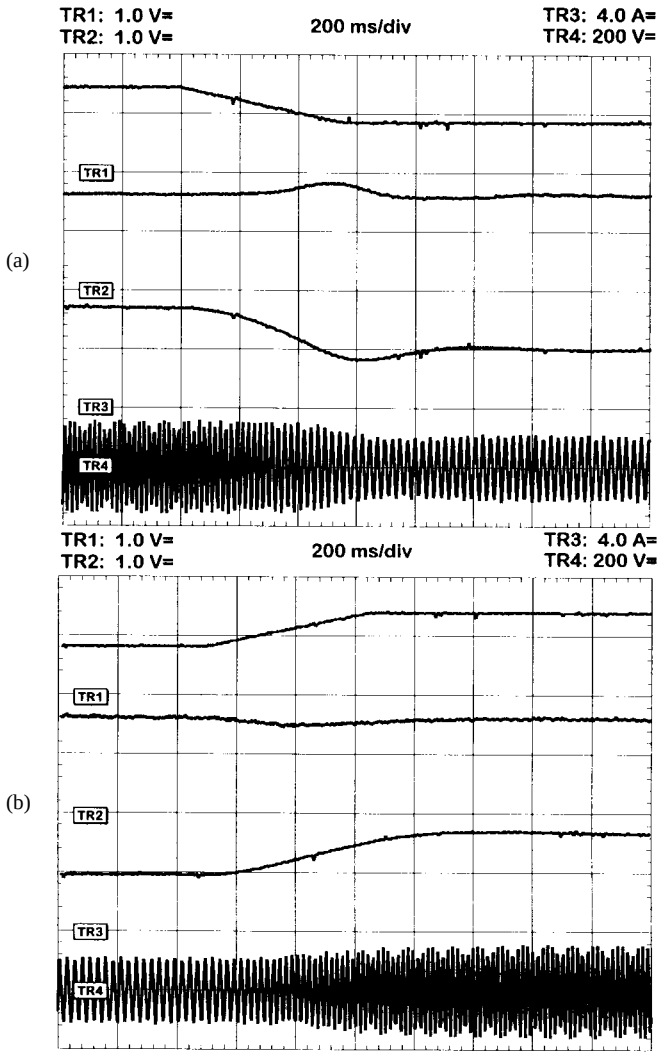

Fig. 5. Experimental transient responses to speed reference changes of the CSI drive based on variable dc-link current operation mode. (a) Ramp decrease from 60 to 40 Hz. (b) Ramp increase from 40 to 60 Hz. (*TR1*: normalized motor speed command $(\omega_{m,\mathrm{ref}})$; *TR2*: CSI modulation index (m_i); *TR3*: dc-link current (i_{dc}); *TR4*: motor voltage (v_{ab}).)

V. Converter and Drive Performance

The power topology is implemented on a 2-kVA laboratory prototype. The induction machine is loaded with a dc generator connected to a bank of resistors. Thus, the overall load features a quadratic power-speed characteristic.

The proposed control strategy is implemented on a digital system based on the TMS320C30 DSP. A user interface running on a PC was used to communicate on-line with the DSP board. This allows various static and dynamic tests to be performed. Experimental tests show that, with a minimum sampling period of 300 μs (maximum sampling frequency f_{sample} of 3.3 kHz), there is enough time to run all the routines. The space-vector technique used in this work assures that the switching frequency f_{sw} is one-half of the sampling frequency and generates the first group of unwanted harmonics around the sampling frequency [13]. A typical switching frequency for medium-power drives is 1 kHz. For convenience, the sampling frequency used is 1.8 kHz. At such a frequency, output frequency synchronization is not required.

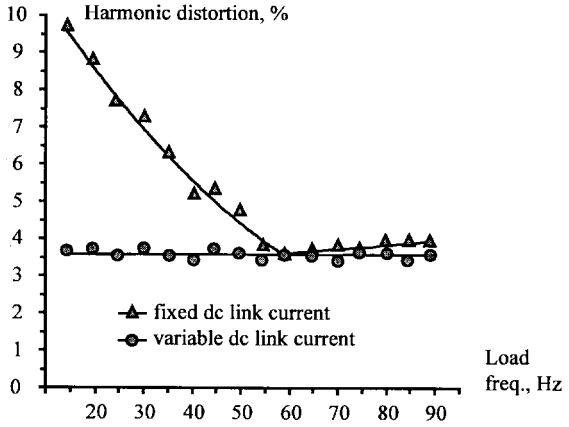

Fig. 6. Motor voltage harmonic distortion (THD_v) as a function of the load frequency (speed) (experimental results for a sampling frequency $f_{\mathrm{sample}} = 1.8$ kHz, filter capacitor $X_{Ci} = 4$ pu, and dc-link inductor $X_{L\mathrm{dc}} = 2$ pu).

A. Voltage and Current Waveforms

Experimental voltage and current waveforms and key spectra for the proposed control scheme are given in Fig. 4, where (a)–(c) shows the motor voltage, CSI ac line current, CSI dc-bus voltage, and dc-link current for the ac drive operating at 30, 60, and 90 Hz. The CSI ac line current spectra is also included in Fig. 4(d) for the same load operating frequencies.

The output (motor) voltage [*TR1* in Fig. 4(a)–(c)], presents a low ripple content. This is due to the filtering action of the load filter capacitor, which is designed to limit harmonic distortion under nominal conditions to typically less than 5% (3.5% is used in this paper). The CSI ac line current [*TR2* in Fig. 4(a)–(c)] is of the PWM type, produced by the space-vector modulation technique applied to the CSI stage. Like the CSI ac line current, the CSI dc-bus voltage [*TR3* in Fig. 4(a)–(c)] is of the PWM type, which minimizes the size of the dc-link inductor.

In the experimental tests, a three-phase 60-μF capacitive filter is used. Simulated results indicate that a 3% harmonic distortion is expected. The value of 3.5% for harmonic distortion is, therefore, used for design purposes.

The spectra of the CSI ac line current for 30, 60, and 90 Hz [Fig. 4(d)] shows that the first group of unwanted harmonics correspond to the sampling frequency of the CSI and are, therefore, located between 1.5–2.0 kHz, regardless of the speed. This is due to the fact that the sampling frequency is maintained constant. In order to eliminate potential resonances between the output capacitor and the motor leakage inductance, the sampling frequency is typically chosen well above this frequency. It should be noted that low-frequency harmonics (fifth and seventh) are also present below 500 Hz [Fig. 4(d)]. These harmonics could possibly be amplified and distort the output voltage. Section V-E analyzes this issue and proves theoretically that the inner voltage closed loop effectively removes these potential resonances.

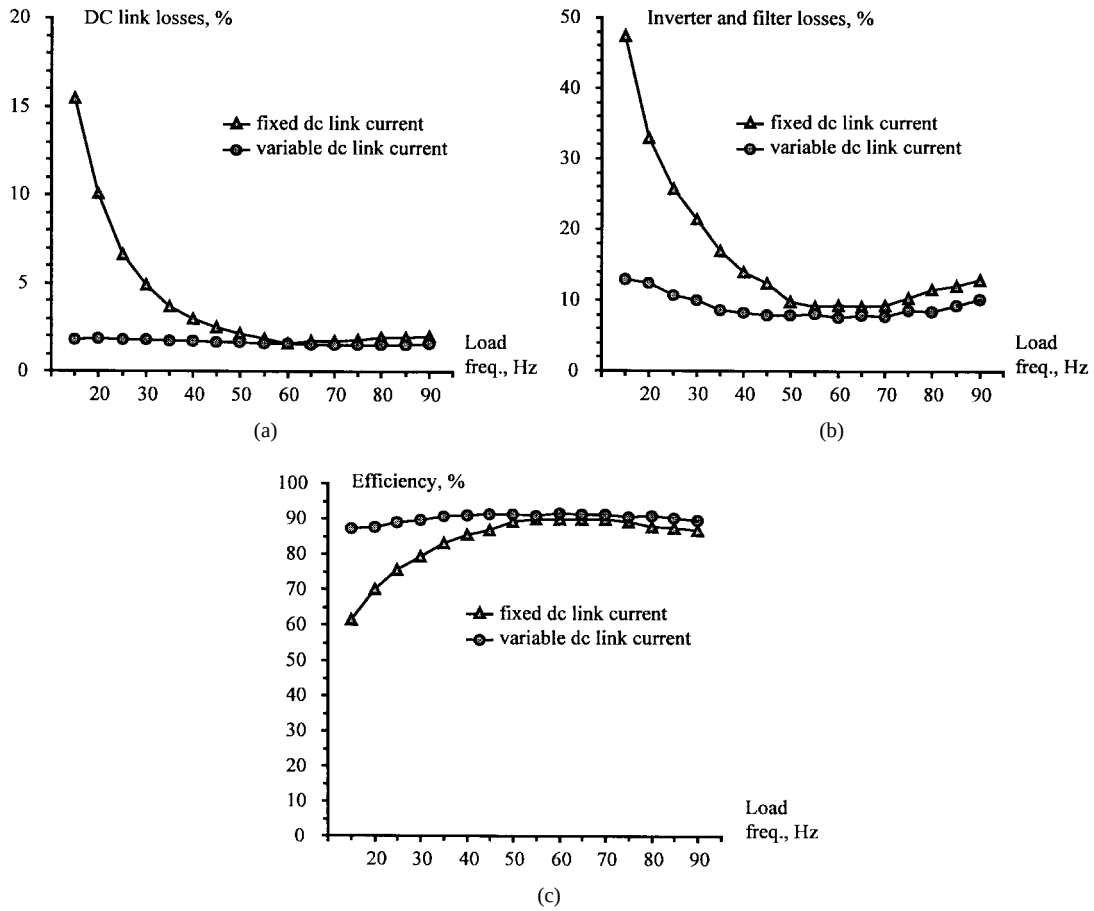

Fig. 7. DC-link and output stage losses as a function of the load frequency (speed). (a) DC-link inductor losses. (b) Inverter and output filter losses. (c) Inverter stage efficiency (including the filter capacitor and dc-link inductor) (experimental results for a sampling frequency $f_{\rm sample} = 1.8$ kHz, filter capacitor $X_{Ci} = 4$ pu, and dc link inductor $X_{L\rm dc} = 2$ pu).

B. Operation of the CSI Modulation Index Control Loop

In order to keep a fixed modulation index for the inverter stage in steady state, the CSI modulation index control loop keeps the dc-link current level to its minimum value (which depends upon the speed and torque load). Fig. 5 shows transient responses to ramp changes in the speed command. From Fig. 5, the following can be seen: 1) the steady-state modulation index of the CSI [*TR2* in Fig. 5(a) and (b)] remains constant (0.8 in this paper) and 2) the dc-link current [*TR3* in Fig. 5(a) and (b)] is adjusted to a minimum value. It should be noted that V_l is a linear function of the speed (a constant V/f scheme is used) and p_l is a quadratic function of the speed (due to the load power/speed characteristic). Therefore, the dc-link current $i_{\rm dc}$ in (5) varies linearly as a function of the speed. Low speeds, therefore, require low dc-link currents (Fig. 5).

Hence, constant modulation index and minimum dc-link current operation are the result of the proposed control strategy, and they have a direct effect on the harmonic content of the motor voltage (due to the constant CSI modulation index) and efficiency of the CSI stage (due to the minimum dc-link current operation mode).

C. Harmonic Distortion of the Motor Voltage

The converter operates at fixed switching frequency, and the control strategy allows the operation of the CSI at constant modulation index. Therefore, an almost constant harmonic content of the CSI ac line current pattern is predicted and, thereby, a constant motor voltage harmonic distortion is expected. Fig. 6 shows for the fixed and variable dc-link current operating modes, the experimental motor voltage total harmonic distortion defined as

$$\mathrm{THD}_v\% = \frac{\sqrt{\sum_{k=2}^{\infty} V_{lk}^2}}{V_{l1}} \cdot 100 \tag{7}$$

where V_{lk} is the kth rms motor voltage harmonic and V_{l1} is the rms fundamental component of the motor voltage. An alternative representation for the total harmonic distortion is given by

$$\mathrm{THD}_v\% = \frac{\sqrt{V_l^2 - V_{l1}^2}}{V_{l1}} \cdot 100 \tag{8}$$

where V_l is the motor rms voltage. In practice, (8) is preferred, since V_l and V_{l1} can be easily obtained from a digital oscilloscope with fast Fourier transform (FFT) capabilities.

As expected, Fig. 6 shows that the variable dc-link current operating mode (or fixed CSI modulation index) allows constant motor voltage harmonic distortion. This feature simplifies the load filter design, since the CSI ac line current spectrum

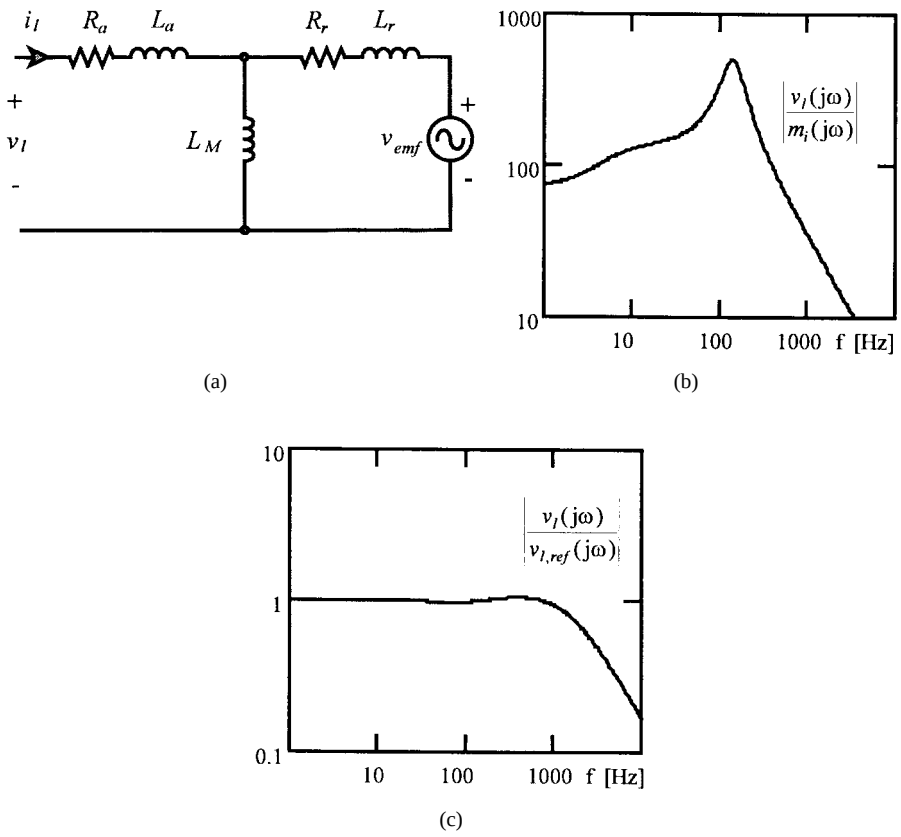

Fig. 8. Transfer functions. (a) Induction machine per-phase equivalent circuit. (b) Motor voltage ($[v_l]$) to modulating waveform ($[m_i]$), open-loop case. (c) Motor voltage ($[v_l]$) to motor voltage reference ($[v_{l,\mathrm{ref}}]$), closed-loop case. 3-hp 208-V three-phase 60-Hz motor with $R_a = 0.6\ \Omega$, $R_r = 0.6\ \Omega$, $L_a = 2.12$ mH, $L_r = 2.12$ mH, $L_M = 53$ mH; converter parameters: $C_i = 100\ \mu$F, $I_{\mathrm{dc}} = 10$ A, $k_{vl} = 0.5$, $T_{vl} = 1$ ms.

remains unaltered, regardless of the load speed and torque. Moreover, the filter can be designed to limit the maximum harmonic distortion to a given value (3.5% in this paper).

D. Converter Losses and Efficiency

For a given load speed and torque, the proposed control strategy minimizes the dc-link current, in order to keep the CSI modulation index constant (0.8 in this paper). The minimization of the dc-link current provides an additional improvement in terms of efficiency over fixed dc-link current operating mode. In this paper, the losses of the dc-link inductor and CSI/output filter are measured for both fixed and variable dc-link current operating modes. Unlike in the variable dc-link operating mode, Fig. 7(a) and (b) shows that, for speeds lower than the nominal one (60 Hz), the losses substantially increase as the speed decreases in the fixed dc-link current operating mode. This effect can be explained as follows.

The dc-link losses are primarily the resistive losses of the dc-link inductor, which are proportional to the internal resistance of the inductor. The CSI losses are basically the conduction losses, which are given by the characteristic power switch turn-on voltage drop. Therefore, both losses are constant and independent of the speed and torque in the fixed dc-link current operating mode. However, the power delivered to the load decreases as the speed decreases; therefore, at low speeds, both losses become a large percentage of the load power [Fig. 7(a) and (b)].

On the other hand, in the variable dc-link current operating mode, both losses decrease as the speed is reduced. Therefore, both losses remain at a relatively constant percentage of the load power [Fig. 7(a) and (b)]. The overall efficiency plot [Fig. 7(c)] of the dc-link inductor and CSI/output filter stages confirms the reduced efficiency of the fixed dc current operating mode as compared to the variable dc current operating mode at low speeds.

E. Effect of Motor Circuit Resonances on Drive Operation

The presence of the output capacitive filter in combination with the induction machine creates resonance frequencies. The per-phase equivalent circuit of the induction machine [Fig. 8(a)] can be represented by the transfer function of (9), shown at the bottom of the page.

$$\frac{v_l(s)}{i_l(s)} = \frac{R_s R_r + s[R_r L_M + R_s(L_r + L_M) + R_r L_s] + s^2[L_r L_M + L_s(L_r + L_M)]}{R_r + s(L_r + L_M)} \tag{9}$$

$$\frac{v_l(s)}{m_i(s)} = I_{\rm dc}\frac{R_sR_r + sL_M(R_r+R_s) + s^2L_M(L_r+L_s)}{R_r + s(L_M + C_iR_rR_s) + s^2C_iL_M(R_r+R_s) + s^3C_iL_M(L_s+L_r)} \tag{10}$$

The capacitive filter behaves as an integrator $(1/C_is)$ and the CSI in combination with the gating generator acts as a current amplifier with an equivalent gain equal to the dc-link current. Therefore, if the dc-link current is considered constant $(i_{\rm dc} = I_{\rm dc}), L_M \gg L_r$, and $L_M \gg L_s$, the motor voltage to modulating waveform transfer function becomes (10), shown at the top of the page.

The magnitude plot of the transfer function of the inverter (motor) output voltage $([v_l])$ to the inverter modulating waveform $([m_i])$ for the open-loop case is given in Fig. 8(b). The plot shows clearly a resonance frequency (f_{ir}) which is associated with the motor leakage reactances. The module of the plot [Fig. 8(b)] shows that, around the resonant frequency, the CSI ac current harmonics are highly amplified, which, in turn, generate high motor voltage harmonics. The approximated value of the resonant frequency is given by

$$f_{ir} = \frac{1}{2\pi\sqrt{C_i(L_s+L_r)}} \tag{11}$$

and falls within the range of frequencies (100–200 Hz) that can be generated by the PWM operation of the inverter. Fortunately, they fall within the bandwidth of the motor voltage loop. The inner control loop used in this paper is a motor voltage controller [12]. It uses a standard PI controller that can be represented by

$$\frac{m_{ik}(s)}{e_{ik}(s)} = k_{vl}\frac{1+sT_{vl}}{sT_{vl}}. \tag{12}$$

Fig. 8(c) plots the resulting closed-loop transfer function of the inverter (motor) output voltage $([v_l])$ to the motor voltage reference $([v_{l,\rm ref}])$. Fig. 8(c) shows that the resonance is effectively attenuated through the action of the voltage control loop. Thus, low-frequency harmonics generated by the PWM operation of the CSI are effectively attenuated. Large capacitive reactive power does not, therefore, flow.

VI. Conclusion

A CSI-based ac induction motor drive topology with a supplemental CSI modulation index control loop has been proposed. The control strategy allows the operation of the inverter at constant modulation index in steady state, regardless of the load speed and torque. The strategy achieves this goal by minimizing the steady-state dc-link current. In addition to the inherent advantages of the CS topology (short-circuit protection, low output dv/dt, and regeneration capabilities), the proposed control scheme adds the following advantages: 1) fixed and reduced motor voltage distortion; 2) minimized dc-bus and switch conduction losses; and 3) elimination of motor circuit resonances through instantaneous output voltage control. Experimental results based on a DSP implementation confirm these features.

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