Current–Source Converter On-Line Pattern Generator Switching Frequency Minimization

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***Abstract*—On-line pulsewidth modulation (PWM) pattern generators for current–source rectifiers and inverters offer a number of control advantages over off-line optimized patterns. However, when implemented using the principles which apply to voltage-source inverter PWM pattern generators, the switching frequency is equal to: 1) the carrier frequency in standard carrier-based implementations and 2) a function of the cycle frequency, sequence of space vectors, and selection of the zero space vector in space vector implementations. This paper shows that this frequency can be reduced to one-half of the respective frequencies. Two pattern generators are investigated: 1) an analog on-line carrier-based technique, namely, the modified dead-band technique and 2) a digital on-line space vector-based technique, where advantage is taken of the extra zero state available in current–source converters. It is shown that the switching frequency reduction is achieved with no penalty in the line current harmonic distortion. Moreover, a significant reduction of ac line current distortion is obtained with the modified dead-band technique for modulation indexes greater than 0.4. The principles of operation of the proposed schemes are explained. Experimental results on a 5-kVA current–source rectifier and a 5-kVA current–source inverter confirm the feasibility and features of the proposed pattern generators.**

***Index Terms*— Current–source converter, minimum switching frequency, on-line control, PWM.**

I. Introduction

TO OPTIMIZE switching patterns for pulsewidth modulation (PWM) current–source converters (CSC's), off-line or programmed patterns are often used [1]–[3]. This method also simplifies the compliance of the gating signals with the special requirements of force-commutated switches in CSC's (rectifiers and inverters), since these requirements can easily be included in the algorithm generating the gating pattern. On-line PWM pattern generators nevertheless offer a number of control advantages over off-line optimized patterns: 1) faster dynamic response; 2) elimination of dc offsets under transient conditions; and 3) continuous and precise control of the ac line current amplitude and phase. However, the switching frequency is usually higher than that of optimized patterns. If implemented by adapting standard voltage-source converter (VSC) pattern generation principles, the switching frequency obtained is equal to: 1) the carrier frequency in standard PWM carrier-based implementations [4], [5] and 2) a function of the cycle frequency, sequence of space vectors (SV's), and selection of the zero SV in SV-based implementations [6], [7].

This paper develops a systematic approach to the selection of the sequence of SV's and zero SV in SV-based techniques. It then shows that the switching frequency can be reduced to one-half of the cycle frequency. The same reduction is obtained for carrier-based techniques. Thus, two types of pattern generators are presented: 1) for carrier-based schemes, a modified dead-band technique is proposed [8], suitable for analog schemes and 2) for SV-based schemes, specific sequences of SV's with optimum zero-SV selection are proposed, suitable for digital schemes.

The principles of operation of the proposed pattern generators are explained (Section II) and implementation details are given (Sections III and IV). Results on 5-kVA prototype units confirm the feasibility and advantages of the proposed pattern generators and illustrate the line current and dc voltage frequency spectra and the corresponding harmonic distortion factors (Sections V and VI). These are obtained in: 1) the rectifier mode for the carrier-based technique and 2) the inverter mode for the SV-based technique.

II. Description and Operation of the Pattern Generators

The main purpose of a pattern generator is to produce gating signals, which applied to a CSC generate line currents $([i]_{abc})$ that track a given set of normalized references $([i_n]_{abc})$ [Fig. 1(a)]. The references are normally generated by an outer control loop (closed or open) according to a given static or dynamic objective. If the purpose of the pattern generator is attained, the converter becomes a current amplifier characterized by:

$$[i]_{abc} = G[i_n]_{abc} i_{\mathrm{dc}} \tag{1}$$

where

- $[i]_{abc}$ actual line currents in abc frame, $[i]_{abc} = [i_a \ i_b \ i_c]^T$;
- $[i_n]_{abc}$ normalized line currents references, $[i_n]_{abc} = [i_{an} \ i_{bn} \ i_{cn}]^T$;
- G gain that depends upon the PWM technique;
- i_{dc} dc bus current.

Note that the line currents are actually PWM waveforms; however, the fundamental tracks the reference up to frequencies of about one-half the carrier (for analog carrier-based implementations) and cycle frequencies (in digital implementations). Also, the neutral is usually not connected; therefore, the line currents $([i]_{abc})$ always add up to 0; therefore, the normalized line current references $([i_n]_{abc})$ must also add up to 0.

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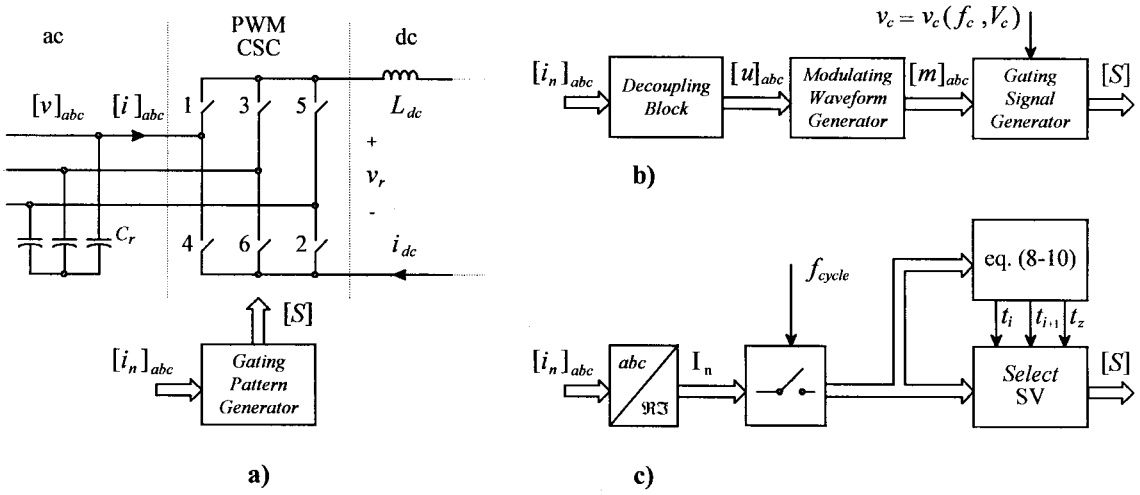

Fig. 1. Generalized CSC and gating pattern alternatives. (a) Power topology. (b) Analog gating pattern implementation. (c) Digital gating pattern implementation.

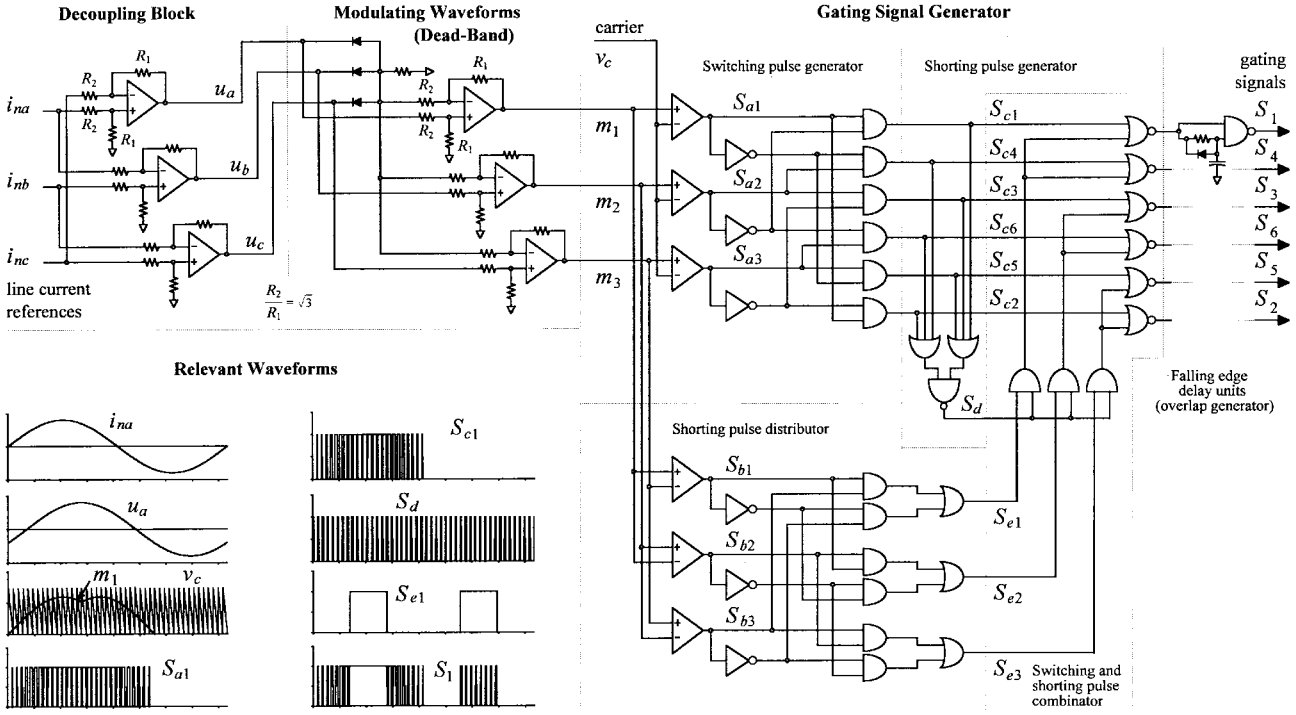

Fig. 2. Gating pattern generator for analog on-line carrier-based PWM current source converters.

In order to properly gate the power switches of a CSC, two main constraints must be met at any time: 1) the ac side draws PWM line currents and, therefore, the ac circuit must be capacitive and must not be short-circuited; this implies that, at most, one top [1, 3, or 5, Fig. 1(a)] and one bottom switch (4, 6, or 2) should be closed at any time, and 2) the dc bus is of the current-source type and, thereby, cannot be opened; therefore, there must be at least one top (1, 3, or 5) and one bottom switch (4, 6, or 2) closed at all times. Note that both constraints can be summarized by stating that, at any time, only one top and one bottom switch must be closed. In this paper, two on-line pattern generators (for analog and digital implementations, respectively) that satisfy the above constraints are investigated.

III. Analog On-Line Carrier-Based PWM Pattern Generator

Since these techniques are carrier-based, they are best suited for analog implementations. The circuit realization of the pattern generator proposed in this paper (Fig. 2) is an extension of [9]. The circuit, as depicted in Fig. 1(b), is implemented in three stages: the gating signal generator, the modulating waveform generator, and the decoupling block.

A. The Gating Signal Generator Stage

The gating signal generator produces the gating signals ($[S] = [S_1 \cdots S_6]^T$) according to a carrier ($v_c = v_c(f_c, V_c)$) and three line-to-neutral modulating waveforms ($[m]_{abc} =$

TABLE I
TRUTH TABLE FOR THE SWITCHING PULSE GENERATOR STAGE (FIG. 2)

S_{a1}	S_{a2}	S_{a3}	Top Switches			Bottom Switches		
			S_{c1}	S_{c3}	S_{c5}	S_{c4}	S_{c6}	S_{c2}
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0
0	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1	0
1	1	0	0	1	0	0	0	1
1	1	1	0	0	0	0	0	0

$[m_1 \ m_2 \ m_3]^T$) [9]. Therefore, any set of signals which, when combined, results in a sinusoidal line-to-line set of signals will satisfy the requirement for a sinusoidal line current pattern. Examples of such modulating signals are the standard sinusoidal, sinusoidal with third-harmonic injection [5], and dead-band-type [8] of waveforms.

The first component of this stage (Fig. 2) is the switching pulse generator, where the signals $S_{ai}(i = 1,2,3)$ are generated according to

$$S_{ai} = \begin{cases} \text{HIGH} = 1, & \text{if } m_i > v_c \\ \text{LOW} = 0, & \text{otherwise} \end{cases} \qquad i = 1,2,3. \quad (2)$$

The outputs of the switching pulse generator are the signals $S_{ci}(i = 1, \cdots, 6)$, which are basically the gating signals of the CSC without the shorting pulses. Table I shows the truth table of S_{ci} for all combinations of their inputs $(S_{ai}, i = 1,2,3)$. It can be clearly seen that at most one top and one bottom switch is ON. This satisfies the first constraint of CSC gating signals as stated before (Section II). In order to satisfy the second constraint, the shorting pulse $(S_d = 1)$ is generated (shorting pulse generator, Fig. 2) when none of top switches $(S_{c1} = S_{c3} = S_{c5} = 0)$ or none of the bottom switches $(S_{c4} = S_{c6} = S_{c2} = 0)$ are gated. Then, this pulse is added (using OR gates) to only one leg of the CSC (either to the switches 1 and 4, 3 and 6, or 5 and 2) by means of the switching and shorting pulse combinator (Fig. 2). The signals $S_{ei}(i = 1,2,3)$ ensure that: 1) only one leg of the CSC is shorted, since only one of the signals is HIGH at any time and 2) an even distribution of the shorting pulse, since $S_{ei}(i = 1,2,3)$ is high for 120° in each period. This ensures that the rms current is equal in all legs. Finally, overlaps (<5 μs) are added as a final stage (falling edge units) to ensure proper commutation of the dc bus current among the top and bottom power switches. This overlap also provides a minimum ON time for the switches.

B. The Modulating Waveform Generator Stage

The modulating waveform generator generates the modulating signals $([m]_{abc})$ out of the voltage signals $([u]_{abc})$. In this paper, a modified dead-band PWM technique is proposed, which unlike the regular dead-band technique proposed for VSI's [8], uses a sawtooth carrier instead of the standard triangular carrier. Fig. 2 shows one alternative to the generation of the dead-band modulating signals. Note that only this stage should be modified according to the alternative modulating waveforms. For instance, for sinusoidal modulating waveforms, this stage could be replaced by voltage followers. Also, the modulating waveforms are instantaneously equivalent in amplitude and phase to the voltage signals $([u]_{abc})$, a basic requirement for on-line implementations.

Theory shows that the line currents $([i]_{abc})$ generated by the CSC and the waveforms $([u]_{abc})$ are related by the following expression:

$$[i_{abc} = \frac{G_{\text{ac}}}{\sqrt{3}V_c}[T][u]_{abc} i_{\text{dc}} \quad (3)$$

where G_{ac} is the ac gain of the PWM technique (e.g., $G_{\text{ac}} = 0.866$ for SPWM [5]), V_c is the amplitude of the carrier waveform (Fig. 2), and

$$[T] = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}.$$

Since $[T]$ in (3) is not diagonal, the line currents are coupled with respect to $[u]_{abc}$; this comes from the fact that each line current is generated from line-to-neutral signals. This feature is particularly undesirable when it comes to designing an external loop to generate the line current references [10], [11]. Therefore, a decoupling block is used to overcome this drawback.

C. The Decoupling Block Stage

The decoupling block can be modeled as a linear transformation given by $[u]_{abc} = [D] \cdot [i_n]_{abc}$ (where $[D]$ is the decoupling matrix to be found, Fig. 1(b)). Therefore,

$$[i]_{abc} = \frac{G_{\text{ac}}}{\sqrt{3}V_c}[T][D][i_n]_{abc} i_{\text{dc}}. \quad (4)$$

If $[D]$ is chosen to be equal to $[T]^T$ and noting that $i_{an} + i_{bn} + i_{cn} = 0$, (4) yields

$$[i]_{abc} = \frac{G_{\text{ac}}}{V_c}[i_n]_{abc} i_{\text{dc}}. \quad (5)$$

Equation (5) shows that the line currents can track the normalized references in a linear and decoupled fashion, as stated in Section II. An alternative to implement the decoupling block is given in Fig. 2. Additional features of the overall circuit over previous realizations are: 1) the decoupling and gating signal generator stages are general approaches and, thereby, they can be used with any on-line carrier-based PWM technique; 2) the carrier waveform can be free-running; and 3) the circuit uses only binary logic to operate, which simplifies its design. Also, the proposed circuit realization (Fig. 2) can be used equally in CS rectifiers (CSR's) and CS inverters (CSI's). In rectifiers, the current references must be synchronized with the ac mains.

TABLE II
CSC STATES AND SWITCH REALIZATIONS

State	ON Switches	i_a / i_{dc}	i_b / i_{dc}	i_c / i_{dc}
1	1, 2	1	0	-1
2	2, 3	0	1	-1
3	3, 4	-1	1	0
4	4, 5	-1	0	1
5	5, 6	0	-1	1
6	6, 7	1	-1	0
7	1, 4	0	0	0
8	3, 6	0	0	0
9	5, 2	0	0	0

IV. DIGITAL ON-LINE SV-BASED PWM PATTERN GENERATOR

Since its introduction [6], [12], the most attractive of digital control methods for VSI's are based on space vector (SV) techniques [4]. The main advantages include: 1) direct implementation of enhanced control strategies (in dq and $\alpha\beta$ frames) and 2) straightforward implementation in digital systems (e.g., DSP's and microprocessors). The proposed SV schemes used for CSC's are adapted from the VSI topology.

The overall performance of the SV-based techniques depend upon the use of the three-degrees-of-freedoms available when implementing the SVM. These are: 1) sequence applied to the selected SV's; 2) selection of the zero SV; and 3) normalized cycle frequency. In this paper, three different sequences are studied, the selection of the zero SV is analyzed, and the influence of the normalized cycle frequency is established.

A. The SV Transformation and CSC SV's

The SV is a complex number that can be associated to any three quantities (not necessarily sinusoidal) which add up to 0. For instance, the SV associated with the ac line currents of a three-phase CSC is given by

$$I = \tfrac{2}{3}(i_a + i_b \cdot e^{j\phi} + i_c \cdot e^{-j\phi}) = I_{\Re} + jI_{\Im} \tag{6}$$

where $\phi = 2\pi/3$, and i_a, i_b, and i_c are the line current components.

Unlike a three-phase VSI, a three-phase CSC has nine valid switch combinations that are named "states." Each state produces a specific set of ac line currents and, thereby, a specific SV can be associated with each one by using (6). Table II shows the nine possible states with their respective ON switches and normalized line currents.

Like the nine states of a CSC, the instantaneous ac line current reference $([i_n]_{abc})$ can be represented by an equivalent SV (I_n). Noting that this vector has a length proportional to the modulation index $(m = \|I_n\|)$ and a constant rotating angular frequency equal to ω for sinusoidal references. The CSC SV's $(I_k, k = 1, \cdots, 9)$ and the line current reference SV (I_n) are represented in a complex plane (Fig. 3).

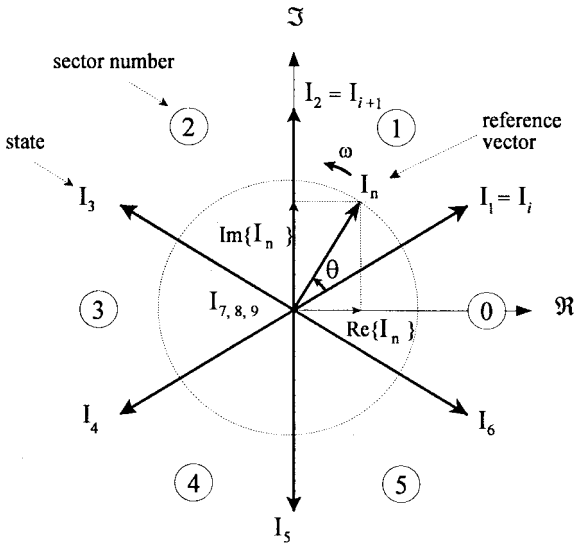

Fig. 3. CSC space vectors and sectors definition.

B. The Space Vector Modulation (SVM)

The objective of the SVM technique, which is also the main objective of the gating pattern generator (Section II), is to approximate the current reference SV (I_n) with the nine SV's $(I_k, k = 1, \cdots, 9)$ available in CSC. However, it has been reported that by approximating the reference SV by only the nearest two nonzero $(I_i$ and $I_{i+1})$ and one zero SV $(I_z = I_7, I_8$, or I_9, Fig. 3), the gain of the technique is maximized [13] and the switching frequency minimized. Thus, if the reference (I_n) is laying between the arbitrary vectors I_i and I_{i+1} (Fig. 3), the following expression can be derived:

$$I_{\text{ref}} \cdot t_{\text{cycle}} = I_i \cdot t_i + I_{i+1} t_{i+1} + I_z \cdot t_z \tag{7}$$

where t_i, t_{i+1}, and t_z for $m \leq 1$ are given by

$$t_i = t_{\text{cycle}} \cdot m \cdot \sin(\pi/3 - \theta) \tag{8}$$

$$t_{i+1} = t_{\text{cycle}} \cdot m \cdot \sin(\theta) \tag{9}$$

$$t_z = t_{\text{cycle}} - t_i - t_{i+1}. \tag{10}$$

Overmodulation $(m \geq 1)$ including six-step operation is not covered in this paper.

C. SV Sequences

The SVM technique selects the vectors to be used and their respective ON times. However, the sequence in which they are used to gate the converter remains undetermined. In this paper, three sequences are studied (Seq_A, Seq_B, and Seq_C, Fig. 4) and their performance evaluated using an harmonic distortion factor (Section V). Note that the evaluation can be done regardless of the selection of the zero SV, due to the fact that the line current waveshape does not depend upon the selected zero vector (I_7, I_8, or I_9, Table II).

D. The Zero SV Selection

It has been reported in the literature that, once the SV sequence is fixed, the selection of the zero SV defines the switching frequency [7]. In steady state, the normalized line current references are usually sinusoidal signals. Therefore,

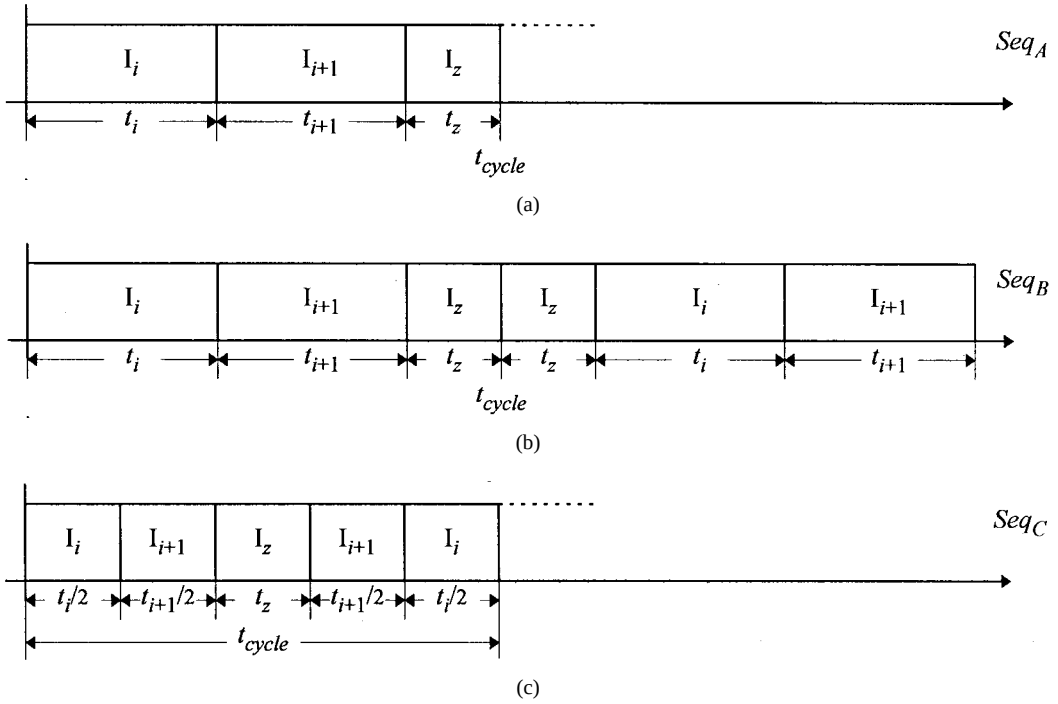

Fig. 4. CSC space vector sequences. (a) Seq_A. (b) Seq_B. (c) Seq_C.

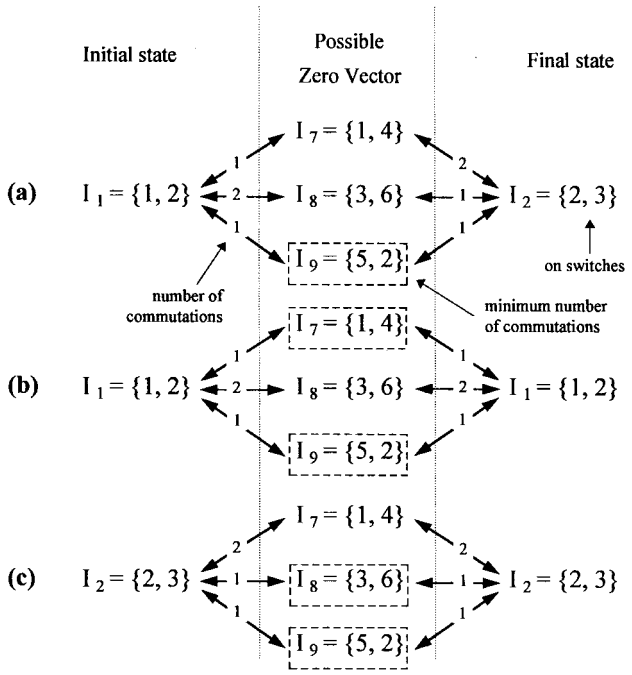

Fig. 5. Possible state transitions in Sector ③ involving a zero SV. (a) Transition: $I_1 \Leftrightarrow I_z \Leftrightarrow I_2$ or $I_2 \Leftrightarrow I_z \Leftrightarrow I_1$. (b) Transition: $I_1 \Leftrightarrow I_z \Leftrightarrow I_1$. (c) Transition: $I_2 \Leftrightarrow I_z \Leftrightarrow I_2$.

TABLE III
ZERO SV FOR MINIMUM SWITCHING FREQ. IN CSC

Sector	I_i	I_{i+1}	I_z
⓪	I_6	I_1	I_7
①	I_1	I_2	I_9
②	I_2	I_3	I_8
③	I_3	I_4	I_7
④	I_4	I_5	I_9
⑤	I_5	I_6	I_8

the line current SV reference (I_n) should describe a circular trajectory with constant angular speed (ω, Fig. 3). Thus, transitions only between adjacent SV's are expected. To illustrate the effect of the zero SV selection, Fig. 5 shows all possible transitions in Sector ①, including the number of switch commutations from one state to another (the number on the branches). Specifically, Fig. 5(a) shows the transition from I_1 to I_2 or I_2 to I_1 (which is possible in all sequences), Fig. 5(b) from I_1 to I_1 (which is possible in Seq_C), and Fig. 5(c) from I_2 to I_2 (which is possible in Seq_C). For instance, let us assume that the initial state is I_1, the final is I_2, and a zero SV is required in between. Fig. 5(a) shows that if either I_7 or I_8 is used, a total of 3 commutations are required; however, if I_9 is used, only 2 commutations are required.

Fig. 5 shows that, for the proposed sequences, I_9 is the zero SV in Sector ① which provides the lowest switching frequency, regardless of the initial and final state. As a generalization, Table III shows the zero vector (I_z) to be used in each sector in order to minimize the switching frequency.

E. Normalized Cycle Frequency Selection

The normalized carrier frequency in three-phase carrier-based PWM techniques is chosen to be an odd integer number multiple of 3 $(f_c = 3 \cdot k, k = 1, 3, 5, \cdots)$. Thus, it is possible to minimize parasitic or nonintrinsic harmonics in the PWM waveforms. A similar approach can be used in the SVM technique to minimize uncharacteristic harmonics. Hence, it is

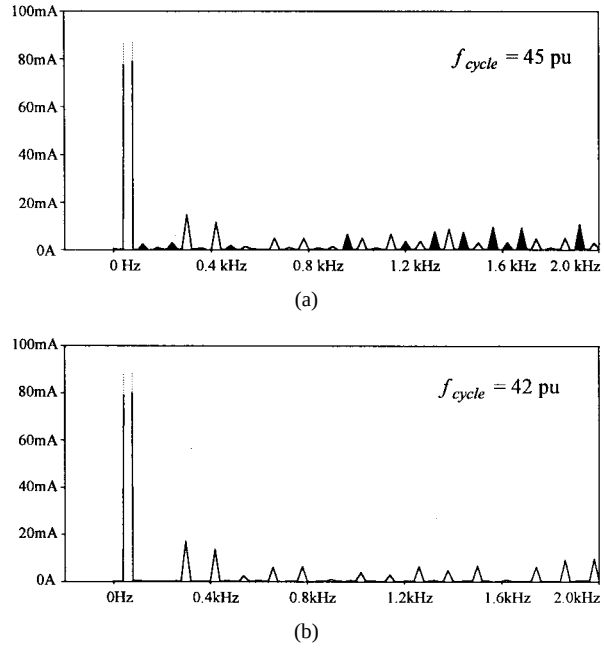

Fig. 6. AC line current spectra for two normalized cycle frequencies ($m = 0.8, f_{\text{base}} = 60$ Hz). (a) $f_{\text{cycle}} = 45$ pu. (b) $f_{\text{cycle}} = 42$ pu (multiple of 6).

TABLE IV
ON-LINE PWM TECHNIQUES COMPARISON

Technique	Category	Switch. freq. (f_{sw})	Ac gain (G_{ac}) [5]
Sinusoidal PWM	analog	f_c	0.866
Third Harmonic Injection	analog	f_c	1.000
Trapezoidal PWM	analog	f_c	1.053
Dead-band PWM [8]	analog	$2/3 \cdot f_c$ - 1	1.000
Mod. Dead-band (Fig. 2)	analog	$1/2 \cdot (f_c + 1)$	1.000
SVM, Seq_A	digital	$3 \cdot (f_{cycle} / 6)$	1.000
SVM, Seq_B	digital	$5 \cdot (f_{cycle} / 12)$ - 1	1.000
SVM, Seq_C	digital	$3 \cdot (f_{cycle} / 6)$ - 1	1.000

found that for the sequences Seq_A and Seq_C, the normalized cycle frequency (f_{cycle}) should be an integer multiple of 6, and 12 for the sequence Seq_B. This is due to the fact that, in order to produce symmetrical line currents, all the sectors, a total of 6, should be equally used in one period. As an example, Fig. 6 shows the line current spectra for two values of f_{cycle} when employing the sequence Seq_A. It can be clearly seen that for $f_{\text{cycle}} = 45$ pu [Fig. 6(a)], additional harmonics are present (the dark areas on the plot), which are not present when $f_{\text{cycle}} = 42$ pu [multiple of 6, Fig. 6(b)].

V. COMPUTER SIMULATION OF THE ON-LINE PATTERN GENERATORS

Analog carrier-based and digital SV-based PWM techniques were investigated through simulation, using the described analog and digital pattern generators, respectively. Table IV shows a comparison of the techniques in terms of switching frequency (f_{sw}) and ac gain (G_{ac}), and Fig. 7 shows the harmonic distortion factor DF_1 (ac factor for second-order

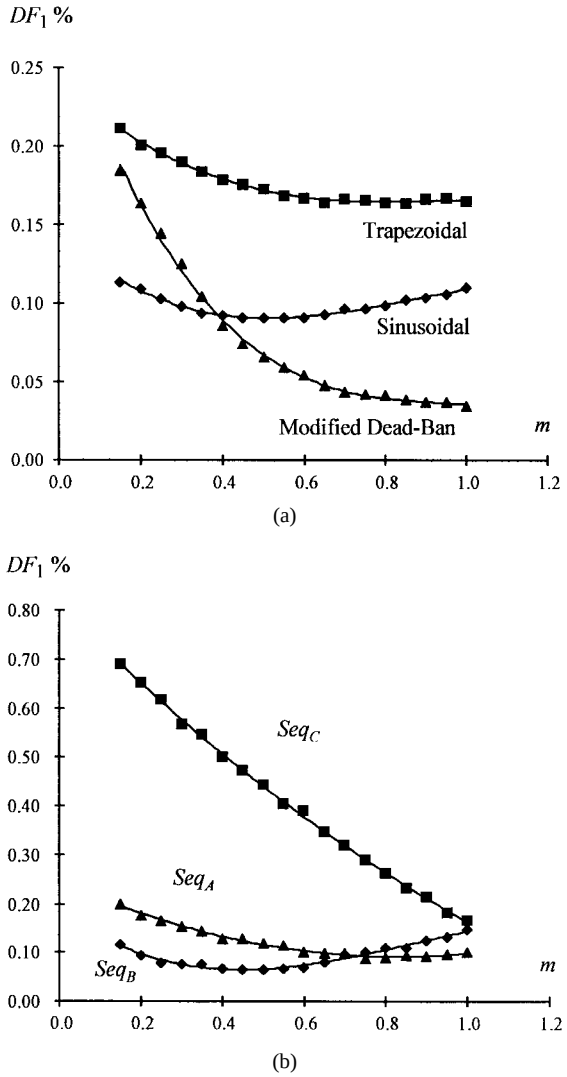

Fig. 7. Harmonic distortion factor for PWM techniques. (a) Analog carrier-based techniques ($f_{\text{sw}} = 1380$ Hz = 23 pu). (b) Digital SV-based techniques (Fig. 4) ($f_{\text{sw}} = 1260$ Hz = 21 pu).

filtering [5]) as a function of the modulation index ($m = ||I_n||$). Two plots are depicted in Fig. 7, since there is not an equal carrier and cycle frequency that satisfy the constraints presented in Section IV *E.* and have a common switching frequency. The distortion factor is defined as

$$DF_1\% = \frac{100}{h_1}\sqrt{\sum_{n=2}^{\infty}\left\{\frac{h_n}{n^2}\right\}^2} \tag{11}$$

where h_n is the rms value of the n^{th} line current harmonic.

The results show that: 1) the proposed modified dead-band technique presents the lowest switching frequency ($\approx 1/2$ of the carrier frequency, Table IV); 2) the lowest ac current distortion for modulation indexes greater than 0.4 (Fig. 7) when compared with standard analog carrier-based PWM techniques; 3) all the digital SV-based PWM techniques present switching frequencies at most one-half of the cycle frequency; and 4) sequence Seq_A presents the lowest distortion factor for modulation indexes greater than 0.8, which is usually the nominal range of values for CSC. Although the distortion

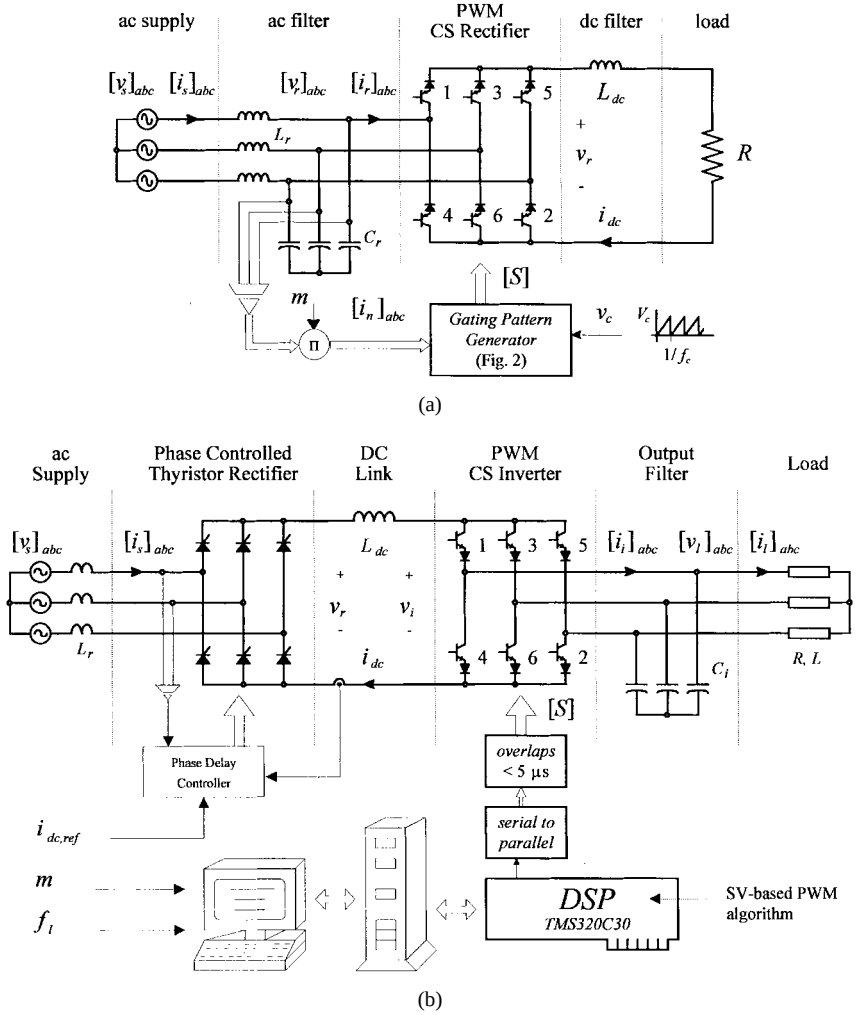

Fig. 8. Experimental setups. (a) PWM CS rectifier using an analog carrier-based gating pattern generator. (b) PWM CS inverter using SVM.

factor is given for two fixed switching frequencies, their shape and relative position are independent of the switching frequency [5].

VI. Experimental Results

The proposed pattern generators were implemented on two 5-kVA prototype units. The results are obtained in: 1) rectifier mode for the carrier-based technique [Fig. 8(a)], where, for simplicity, the capacitor voltages are used as the line current templates and 2) inverter mode for the SV-based technique [Fig. 8(b)], where the DSP sets internally the line current references for a given CSI modulation index and load frequency. The Appendix shows the component and parameters values used in both setups. Fig. 9 shows the experimental waveforms for the CS rectifier in Fig. 8(a) and modulated with the proposed modified dead-band carrier-based scheme (Fig. 2), and Fig. 10 shows the experimental waveforms for the CS inverter in Fig. 8(b) and modulated with the SV-based PWM scheme (Seq_A, Fig. 4). Sequences Seq_B and Seq_C were also implemented, but experimental waveforms are not included.

These experiments show that the main claims for the proposed gating pattern generators have been substantiated. These are: 1) CSC can be on-line PWM modulated using any analog carrier-based PWM technique, as long as the modulating signals are on-line physically realizable; 2) the switching frequency of CSC is reduced to $1/2\cdot(f_c+1)$ for the proposed dead-band carrier-based scheme [Fig. 9(b)], and to $1/2\cdot f_{\text{cycle}}$ for the SV-based scheme [Fig. 10(b)]; and 3) the modified deadband and Seq_A of the SV-based techniques present the lowest distortion factors for high modulation indexes. Also, it is verified that the PWM waveforms present their first set of low-frequency harmonics around the carrier frequency for the analog scheme [Fig. 9(e) and (f)] and around the cycle frequency for the digital scheme [Fig. 10(e) and (f)]. This last feature verifies the low harmonic distortion factors obtained through simulation in Fig. 7.

VII. Conclusion

Two on-line PWM gating pattern generators for three-phase current–source converters have been proposed. These are: 1) a technique best suited for analog control schemes, which uses three dead-band modulating and a sawtooth carrier signal and 2) one best suited (Seq_A) for digital control schemes, based on space vectors. Both approaches reduce the switching frequency of the power valves of the converter to almost one-half of the carrier frequency, in carrier-based schemes, and one-half of the cycle frequency in space vector-based digital schemes. This reduction is achieved with no penalty on the line

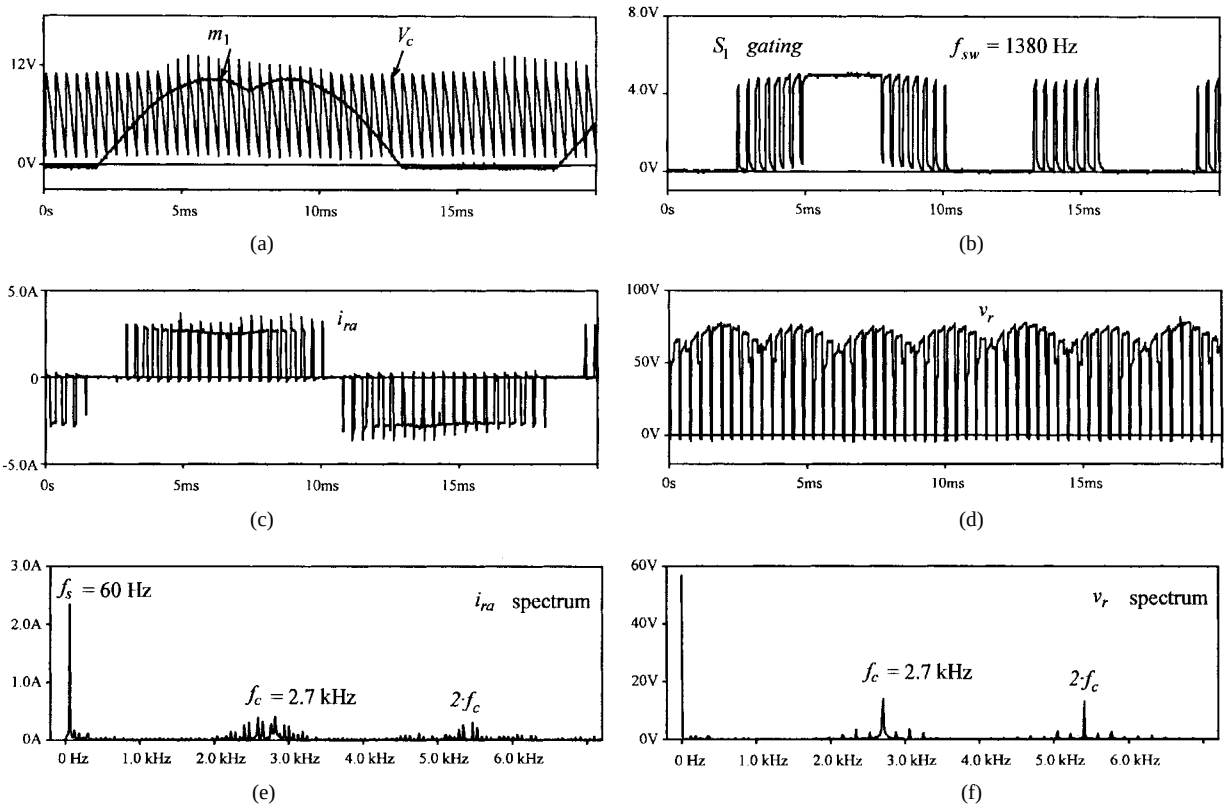

Fig. 9. Experimental results for the modified dead-band PWM carrier-based scheme [Fig. 8 (a)], $m = 0.8, f_{\rm sw} = 23\ {\rm pu} = 1380\ {\rm Hz}, f_c = 45\ {\rm pu} = 2.7\ {\rm kHz}$). (a) Modulating signal (m_1) and carrier waveform (v_c). (b) Gating signal for switch 1 (S_1). (c) Rectifier input current (ir_a). (d) Rectifier dc bus voltage (v_r). (e) Rectifier input current spectrum (ir_a). (f) Rectifier dc bus voltage spectrum (v_r).

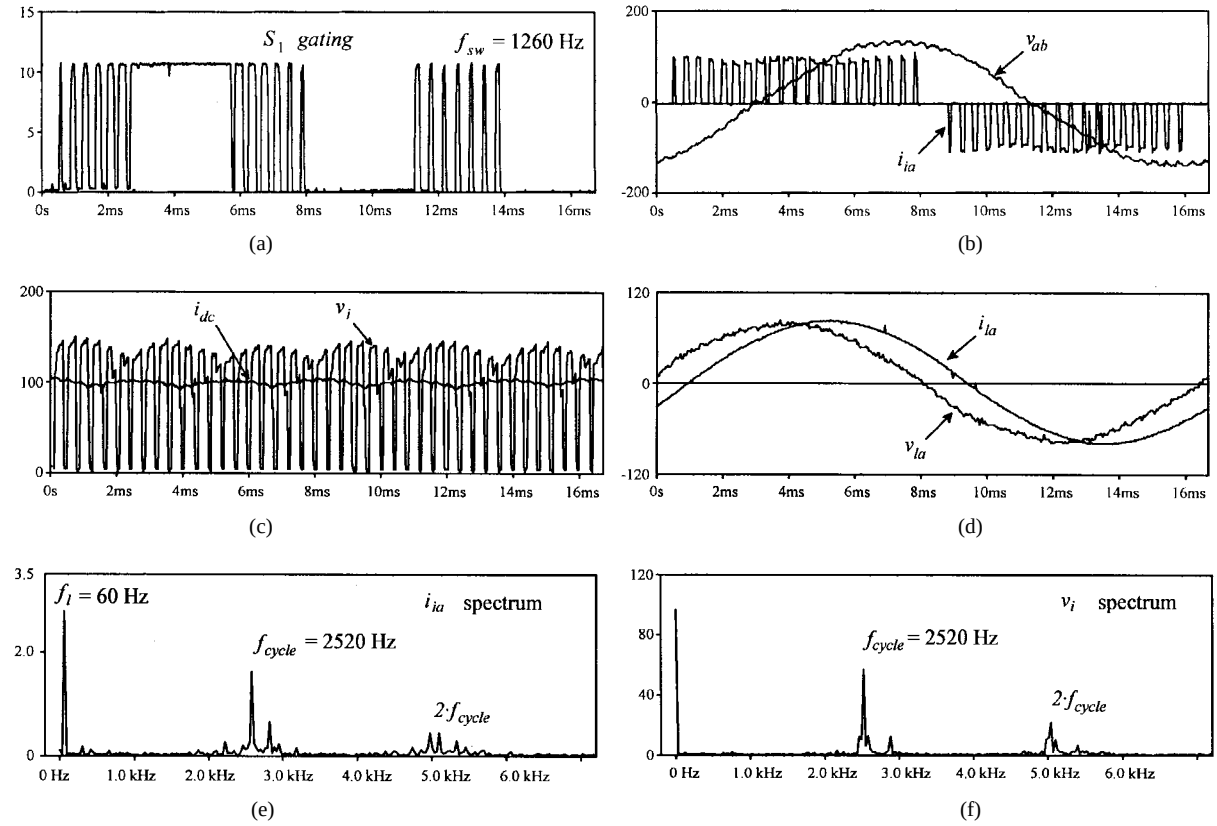

Fig. 10. Experimental results for the SV-based PWM-based scheme [Fig. 8(b)]. $m = 0.8, f_{\rm sw} = 21\ {\rm pu} = 1260\ {\rm Hz}, f_{\rm cycle} = 2520\ {\rm Hz}, Seq_A$-Fig. 4). (a) Gating signal for switch 1 (S_1). (b) CSI line current (i_{ia}) and line load voltage (v_{ab}). (c) DC bus voltage (v_i) and current (i_{dc}). (d) Load phase current (i_{la}) and phase voltage (v_{la}). (e) CSI line current spectrum (i_{la}). (f) DC bus voltage spectrum (v_i).

current harmonic distortion. Moreover, the proposed analog technique presents the lowest one for modulation indexes greater than 0.4. Additional features of the schemes are: 1) they can be used in both current–source rectifiers and inverters without modification; 2) the analog pattern generator circuit realization can be used to implement any on-line carrier-based PWM technique (e.g., SPWM, trapezoidal); and 3) the analog pattern generator circuit realization can be operated with a free-running carrier signal.

APPENDIX
COMPONENTS VALUES FOR EXPERIMENTAL TESTS

Parameter		Value
Current-Source Rectifier Circuit, Fig. 8(a)		
m	nominal CSR modulation index	0.8 pu
f_c	carrier frequency	2.7 kHz
V_c	carrier amplitude	10 V
v_{ab}	supply line voltage	220 V
f_s	supply frequency	60 Hz
C_r	input filter capacitor	50 μF
L_r	input filter inductor	7 mH
$L_{\rm dc}$	dc link inductor	30 mH
R	load resistance	20 Ω
Current-Source Inverter Circuit, Fig. 8 (b)		
m	nominal CSI modulation index	0.8 pu
v_{ab}	load line voltage	220 V
f_l	load frequency	60 Hz
$f_{\rm cycle}$	cycle frequency♣	2.52 kHz
R	load resistance	17 Ω
L	load inductance	35 mH
$i_{\rm dc,ref}$	dc link current reference	9 A
$L_{\rm dc}$	dc link inductor	30 mH
C_i	load filter capacitor	35 μF

♣ Experimental tests show that with a minimum sample period of 60 μs, there is enough time to run the totality of routines required by the DSP system. Thus, the maximum cycle frequency is around 16.7 kHz.

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REFERENCES

[1] H. Karshenas, H. Kojori, and S. Dewan, "Generalized techniques of selective harmonic elimination and current control in current source inverters/converters," *IEEE Trans. Power Electron.*, vol. 10, pp. 566–573, Sept. 1995.

[2] P. Enjeti, P. Ziogas, and J. Lindsay, "Programmed PWM technique to eliminate harmonics: A critical evaluation," *IEEE Trans. Ind. Applicat.*, vol. 26, pp. 302–316, Mar./Apr. 1990.

[3] P. Enjeti, P. Ziogas, and J. Lindsay, "A current source PWM inverter with instantaneous current control capability," *IEEE Trans. Ind. Applicat.*, vol. 27, pp. 893–643, May/June 1991.

[4] J. Holtz, "Pulsewidth modulation—A survey," *IEEE Trans. Ind. Electron.*, vol. 39, pp. 410–420, Oct. 1992.

[5] M. Boost and P. Ziogas, "State-of-the-art carrier PWM techniques: A critical evaluation," *IEEE Trans. Ind. Applicat.*, vol. 24, pp. 271–280, Mar./Apr. 1988.

[6] J. Holtz, P. Lammert, and W. Lotzkat, "High-speed drive system with ultrasonic MOSFET PWM inverter and single-chip microprocessor control," *IEEE Trans. Ind. Applicat.*, vol. IA-23, pp. 1010–1015, Nov./Dec. 1987.

[7] V. Stefanovic and S. Vukoswic, "Space-vector PWM voltage control with optimized switching strategy," in *Conf. Rec. IEEE-IAS'92*, 1992, pp. 1025–1032.

[8] V. Agelidis, P. Ziogas, and G. Joós, "Dead-band PWM switching patterns," in *Conf. Rec. IEEE-PESC'92*, 1992, pp. 427–434.

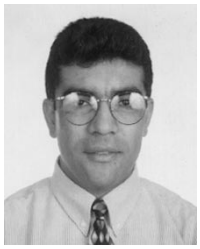
[9] J. Espinoza and G. Joós, "On-line generation of gating signals for current source converter topologies," in *Conf. Rec. IEEE ISIE'93*, 1993, pp. 674–678.

[10] X. Wang and B. Ooi, "Real-time multi-DSP control of three phase current-source unity power factor PWM rectifier," *IEEE Trans. Power Electron.*, vol. 8, pp. 295–300, July 1993.

[11] X. Wang and B. Ooi, "Unity PF current-source rectifier based on dynamic trilogic PWM," *IEEE Trans. Power Electron.*, vol. 8, pp. 288–294, July 1993.

[12] H. Van der Broeck, H. Skudelny, and G. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," in *Conf. Rec. IEEE IAS'86*, 1986, pp. 244–251.

[13] F. Jenni and D. Wueest, "The optimization parameters of space vector modulation," in *Conf. Rec. EPE'93*, 1993, pp. 376–381.



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